中国科学院上海高等研究院
SHANGHAI ADVANCED RESEARCH INSTITUTE, CHINESE ACADEMY OF SCIENCES

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A Novel Cavity BPM Electronics for SHINE Based on RF Direct Sampling and Processing

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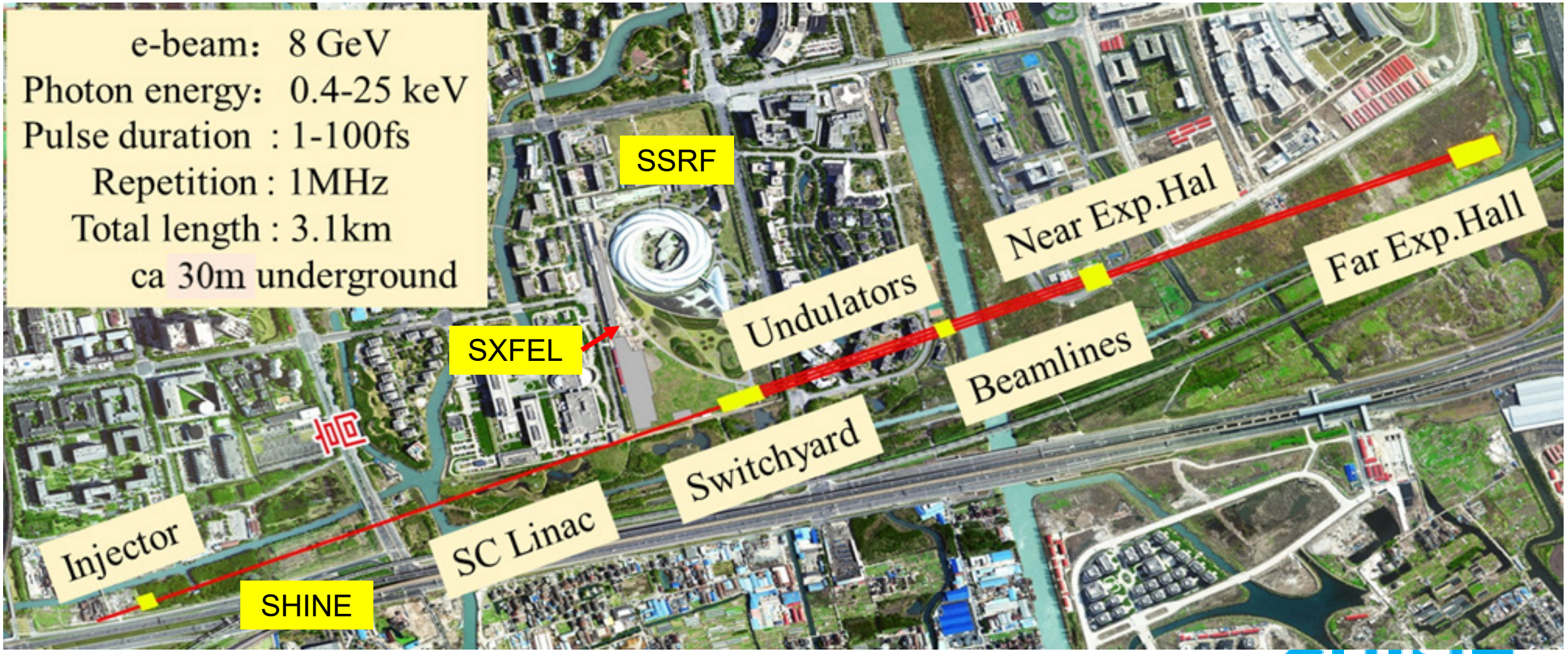
SHINE

Overview

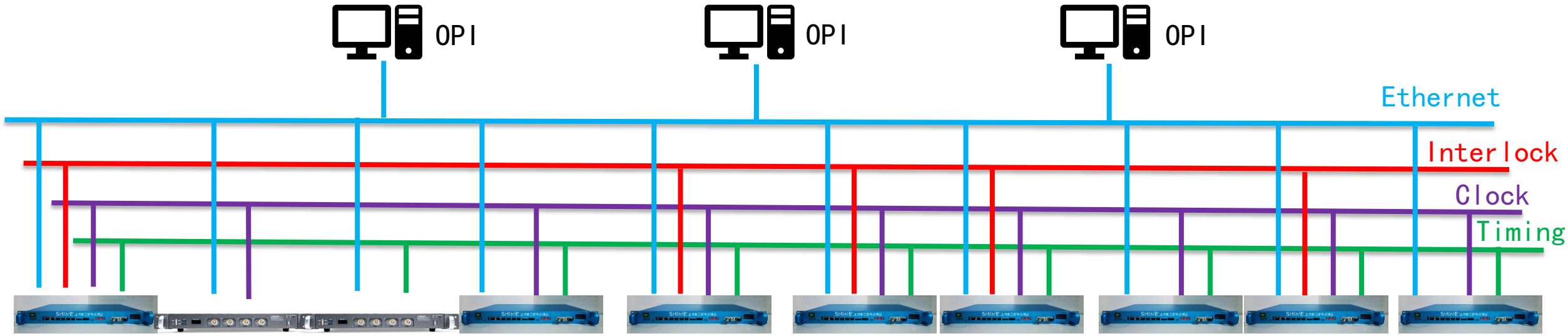
- SHINE and Cavity BPM electronics
- Requirements of RF Direct sampling Electronic(RFDE)
- The RFDE for SHINE cavity BPM
- Performance evaluation and FPGA implementation
- Is it time to use the RFDE in large-scale?

SHINE Introduction



SHINE

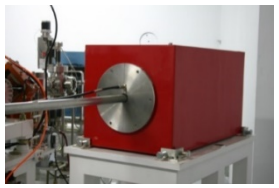
SHINE Beam Diagnostics Using Electronics

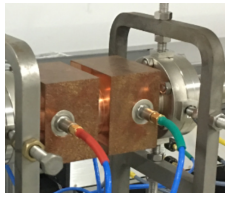


RF Front-end | RF Front-end | RF Front-end | RF Front-end | RF Front-end | RF Front-end | RF Front-end | RF Front-end | RF Front-end

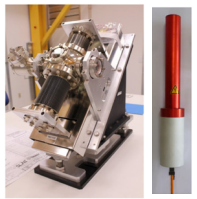

Stripline BPM


ICT


FaradyCup

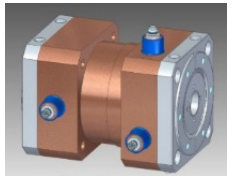

RF-BAM

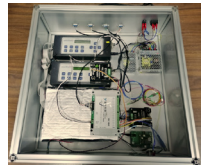

FBL


Wire Scanner


ColdBPM


CSR-BLM


CavityBPM


EO-BAM

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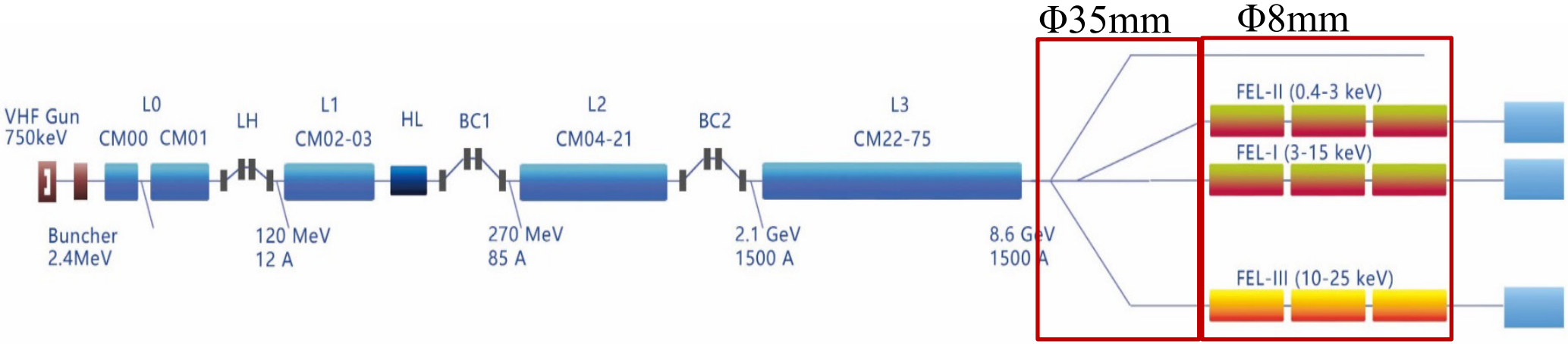
SHINE BPMs



Injector and sections between cryomodule SBPM Resolution

10 um@100 pC

Cryomodules in LINAC Cold-BPM Resolution

50 um@100 pC

Beam distributor & FEL CBPM Resolution

Φ35mm, 1μm@100 pC ·±1mm

Φ8mm, 200 nm@100pC·±100μm

Electronics

Required Relative error ≦1.0×10^{-3}

SHINE Cavity BPM

- The central frequency of Φ35mm is 3520.87MHz(same as RF-BAM).
- The central frequency of Φ8mm is 5254.2MHz

Parameters	Position cavity	Reference cavity
Resonant frequency / MHz	**3520.87**	**3520.87**
Cavity radius / mm	51.9	32.6
Cavity length / mm	9	4.5
Decay time / ns	200	200
Bandwidth / MHz	1.59	1.59
Loaded Q	2212	2212
Qext	3245	5869
Q0	6951	3550
Normalized shunt impedance	0.175@1mm	50.65
Sensitivity /V/nC	0.575@1mm	7.26

Φ35mm

Parameters	Position cavity	Reference cavity
Resonant frequency / MHz	**5254.2**	**5254.2**
Cavity radius / mm	34.8	21.8
Cavity length / mm	9	5
Decay time / ns	200	200
Bandwidth / MHz	1.59	1.59
Loaded Q	3301	3301
Qext	5663	1268
Normalized shunt impedance	0.56@1mm	82.6
Sensitivity /V/nC	1.15@1mm	9.4

Φ8mm

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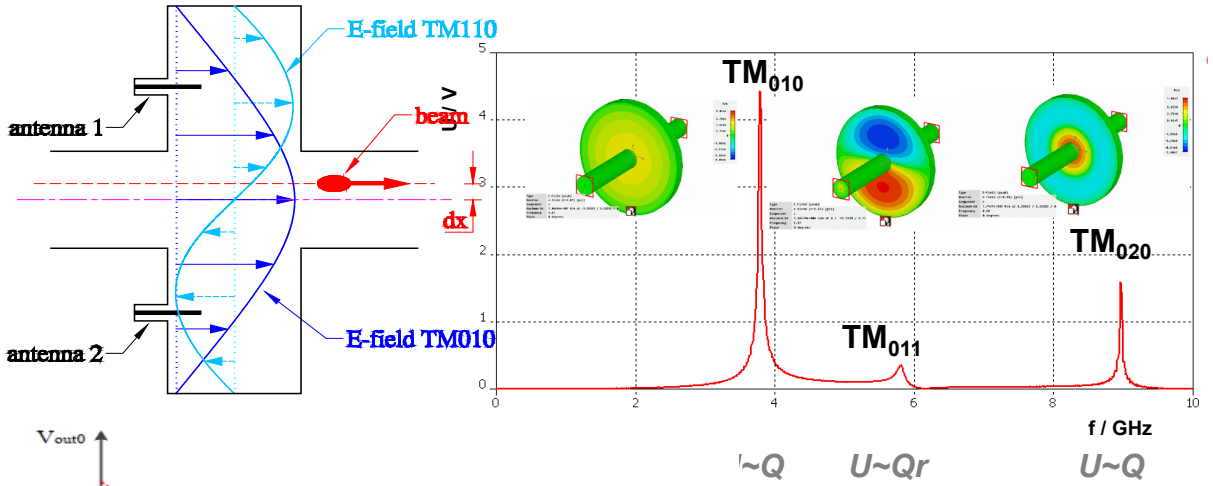
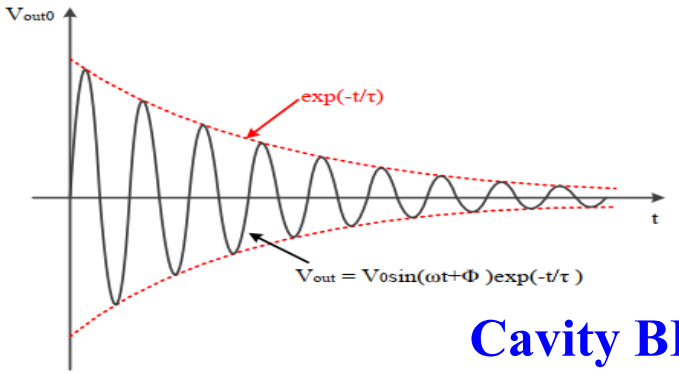
Cavity BPM System

- Cavity BPM generates narrow bandwidth at high frequency signal when beam passes through



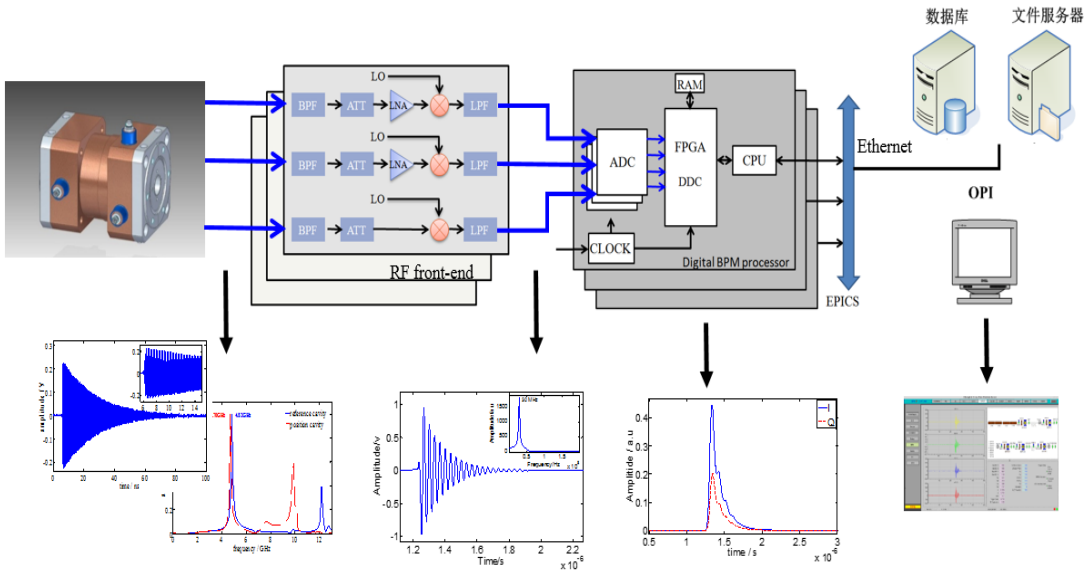


$q, Vout\ 110 \propto qx$

Courtesy D. Lipka, DESY

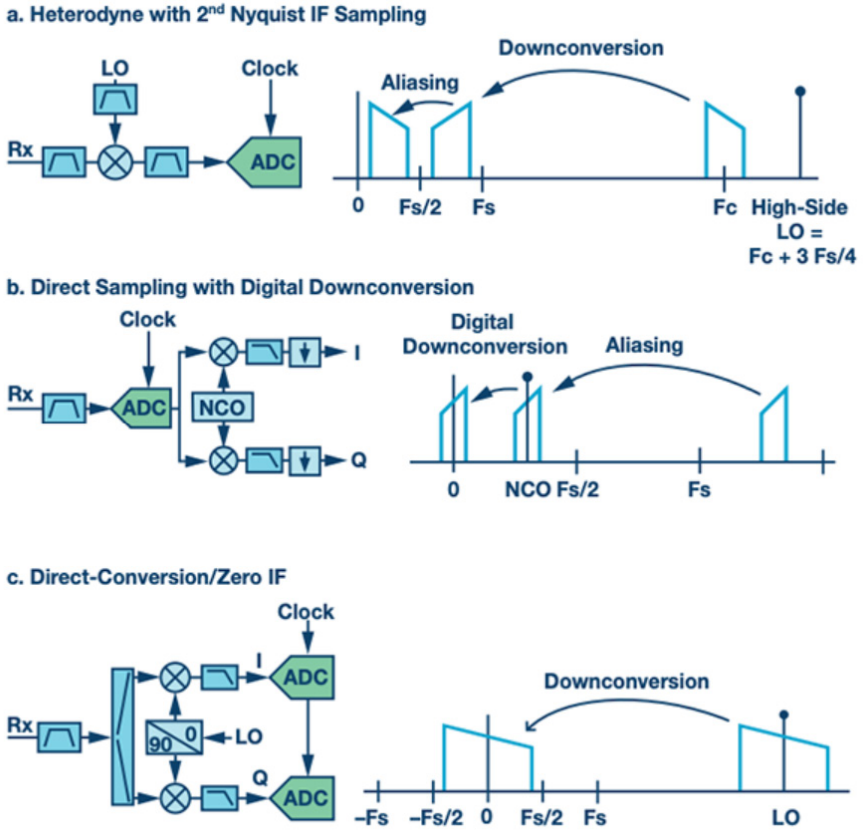
Cavity BPM Signal

- Cavity BPM system including pickup, RF front-end, signal processor



Cavity BPM System

Architecture of Cavity BPM Electronics



Electronic Structure

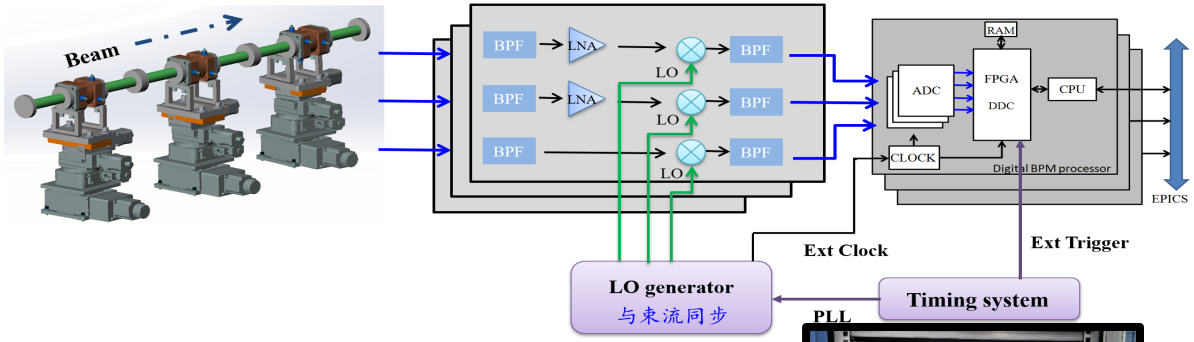
	Benefits	Challenges
Heterodyne	trusted and high performance Optimum spurious noise	Complicate, large physical footprint.
Direct Sampling	No mixing Practical at L-, S-, C-band Flexible application	ADC input bandwidth ENOB
Direct-conversion	Easier low-pass filter Lower ADC requirements Simplest digital processing	I/Q balance LO leakage DC and 1/f noise One more ADC

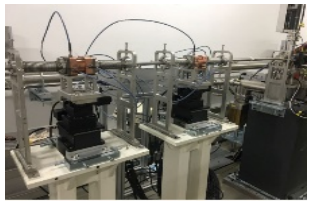
Peter Delos, A review of wideband RF Receiver architecture options, Analog Devices, Inc

SHINE

SXFEL Cavity BPM System

- Heterodyne structure in SXFEL





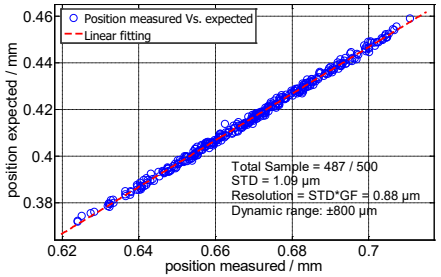
Pickup

RF front-end in tunnel

LO synthesizer
Down converter
DBPM

Components	Parameters
Pickup	Central Frequency: 4681 / 4689 / 4685 MHz Q_L / Decay time: ~ 5000 / 320 ns Sensitivity: 0.5 V / nC · mm / 5.4 V / nC
RF front-end	Dynamic range:± 2mm @ 500pC NF @ position cavity: 12 dB NF @ reference cavity: 25 dB IF SNR = 90 dB @ 500 pC
DBPM	ADC bits：16 Sampling rate: 119 MSPS ADC band width: 650 MHz Processing rate :50Hz

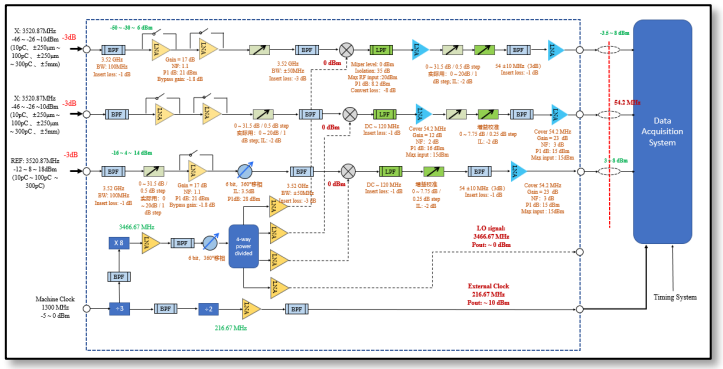
SXFEL DBPM



880nm@500pC ·±800 μm

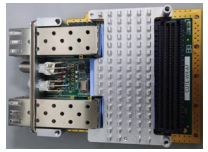
SHINE Cavity BPM Electronics

- Heterodyne structure, IF = 54MHz, fs=866.67MHz
- DBPM:
  - 1U Stand alone structure containing SoC FPGA carrier board, high speed ADC board, White Rabbit timing board
  - 4 RF input channels, maximum sampling rate **1GSPS, 14bits, 2GHz band width, ENOB=10.8@50Hz Fin**

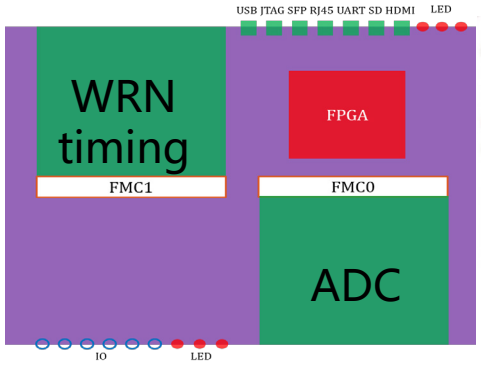


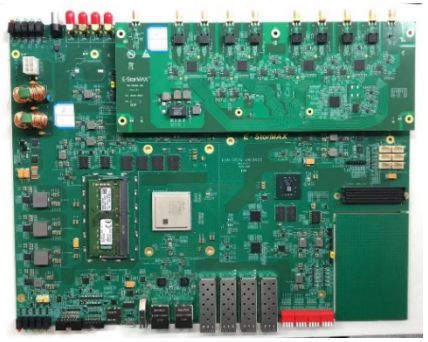
SHINE Cavity BPM System

BPM Electronic



White Rabbit Board





FPGA board and ADC board

Parameters	value
Channels	4
ADC bits	14
Bandwidth	2GHz
Max ADC rate	1GSPS
FPGA	Xilinx ZCU15EG
Clock	Ext./Int.
PL DDR4	8GB
Trigger	Ext./Self/Period
Interlock	Lemo
SFP	×4, UDP&Aurora
User GPIO	×16,SMA&PMOD
Software	Linux/EPICS

SHINE Generic Processor

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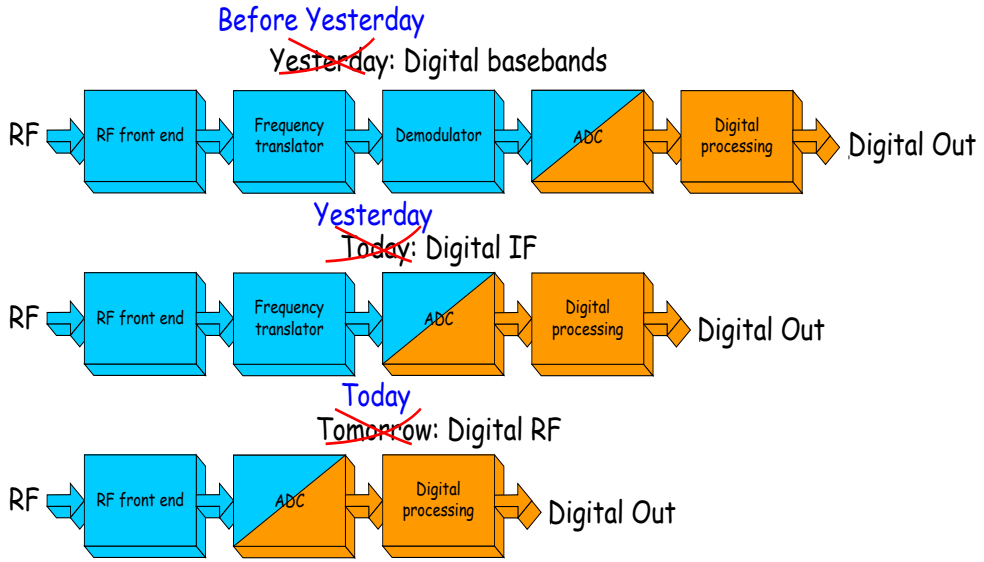
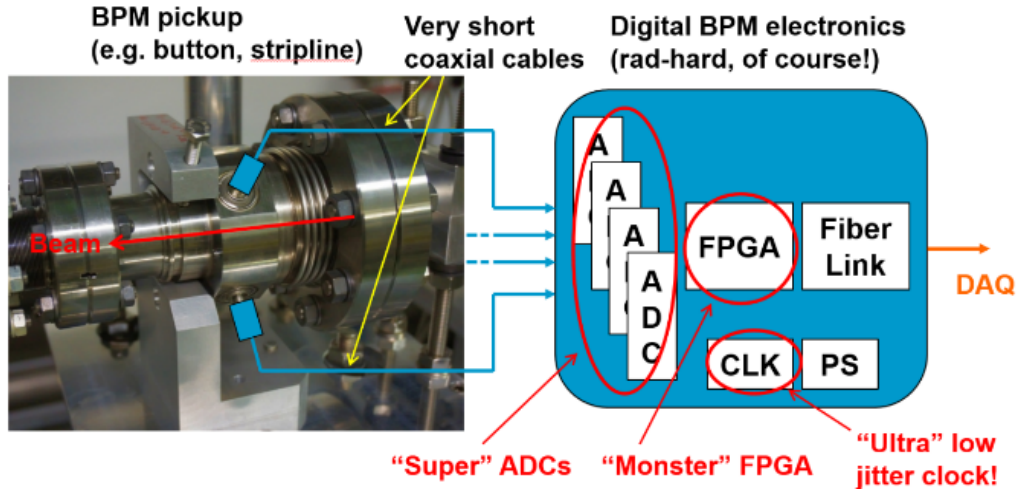
The Development of Electronics

- Moving signal processing from analog to digital is a long-term goal

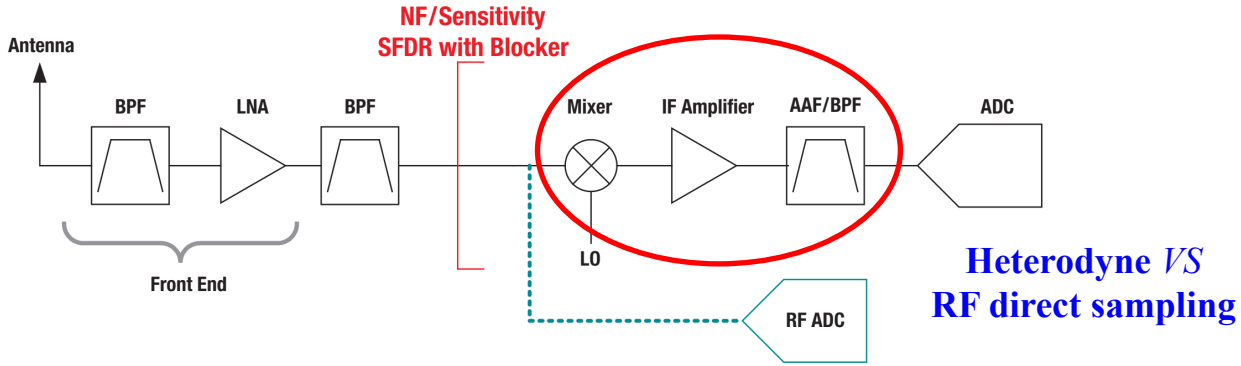


The Ideal BPM Read-out Electronics!?



Courtesy of Hermann Schmickler, CERN, IBIC 2015

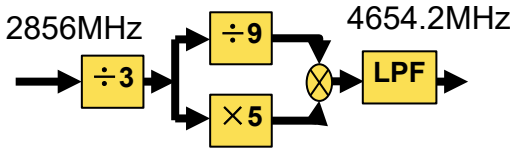
Electronic Development



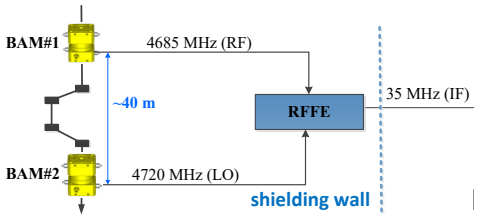
Heterodyne *VS*
RF direct sampling

Benefits from RF Direct Sampling

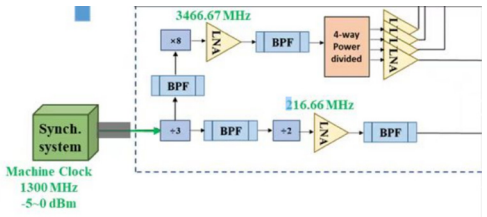
- Simplify electronics: no LO synthesizer and mixing module
- Improve system sensitivity: introduced signal loss and noise during down conversion is avoided
- Smaller system size and reduce power consumption



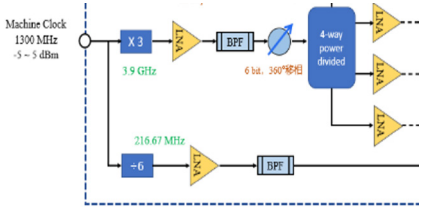
SXFEL CBPM LO synthesizer



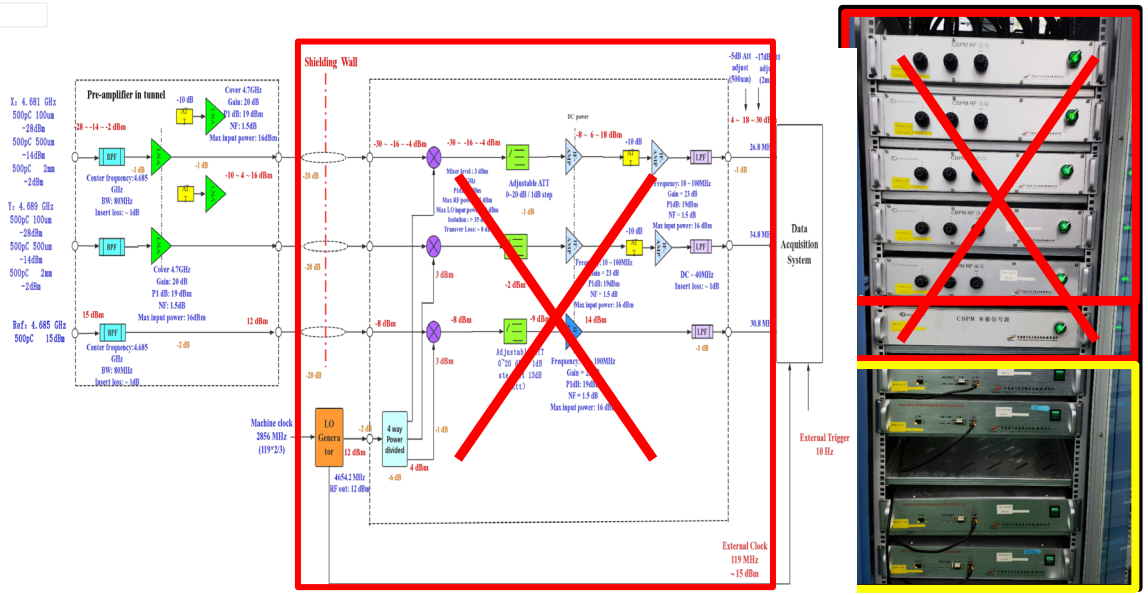
SXFEL Double cavity



SHINE Φ35 CBPM LO



SHINE Φ8 CBPM LO



SXFEL Cavity BPM Electronic

Review of RFDE in Beam Signal Processing

- Applications: LLRF, TFB, BAM, Digitizer
- ADC boards sampling rate < 1GHz, band width < 2.5GHz
- XILINX RFSoC demo boards with multi number high speed ADC and DAC

	ADC Band Width	Sampling Rate	Bits	Interface
ADS5474	1.4GHz	400MHz	14	LVDS
AD9433	760MHz	125MHz×4	12	CMOS
ADS42LB69	900MHz	250MHz	16	LVDS
ADC12D500RF	2.4GHz	500MHz	12	LVDS
ZCU111		4GHz×8	12	RFSoC
ZCU216	6GHz	2.5GHz×16	14	RFSoC

Courtesy Z.Geng, DESY, THP102, LINAC08

Courtesy T. Nakamura, JASRI/Spring-8, THPC128, EPAC08

Courtesy Zhou Zeran, NSRL, Vol.22, No.7 Jul., 2010, High Power Laser and Particle Beams

Courtesy Y.Okada, KEK, WE5PFP088, PAC09

Courtesy J. Zink, DESY, TUPP002, IBIC2019; THOA02, IBIC2018

Courtesy D. B. Li, IHEP, MOPAB390, IPAC2021

Courtesy E. Cicek, KEK, WEPAB297, IPAC2021

Courtesy O.Manzhura, KIT, MOPOPT017, IPAC2022

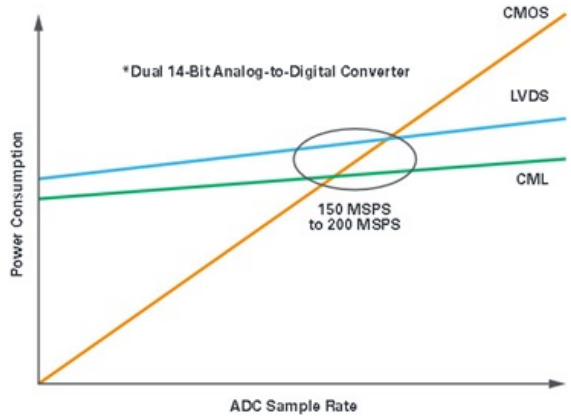
Courtesy P.Baeta, PSI, WE2C4, IBIC2022

Courtesy J. Weber, LBNL, WEPP16, IBIC2020

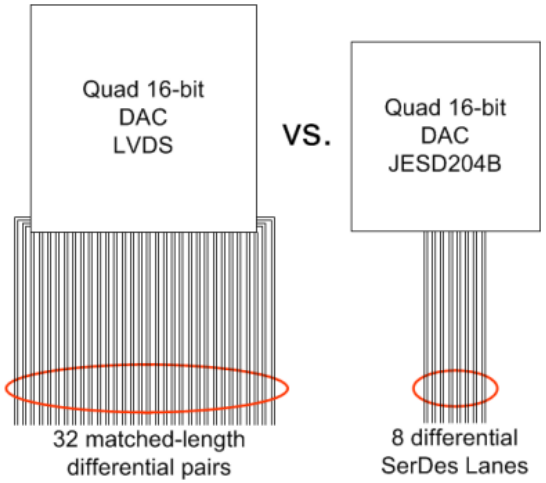
ADC Performance

- ADCs band width > 6GHz, sampling rate > 2GHz, resolution ≧ 12bits
- High speed serial data link between converters and receivers(JESD204B 12.5Gbps)

Type	Sampling Rate	Bits	Band width	Channels	JESD LANE	Year
AD9689	2.6GHz	14 bit	9GHz	2	8	2017
AD9208	3GHz	14bit	9GHz	2	8	2017
AD9213	10.25GHz	12bit	6.5GHz	1	16	2020
AD9209	4GHz	12bit	8GHz	4	8	2021
ADC12DJ5200SE	5.2G	12	6.3G	2	16	2023
ADC12DL3200	3.2G	12	8G	2	48对LVDS 1.6Gbps	2018
AFE7444	3GHz	14bit	6GHz	4	8	2019
AFE7900	3GHz	14bit	7.4GHz	6	8*29.5Gbps	2022
AFE7950	3GHz	14bit	12GHz	6	8*29.5Gbps	2023



https://www.analog.com/en/technical-articles/what-is-jesd204-and-why-should-we-pay-attention-to-it.html

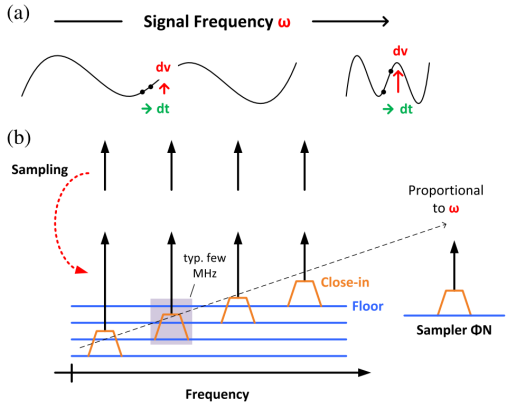


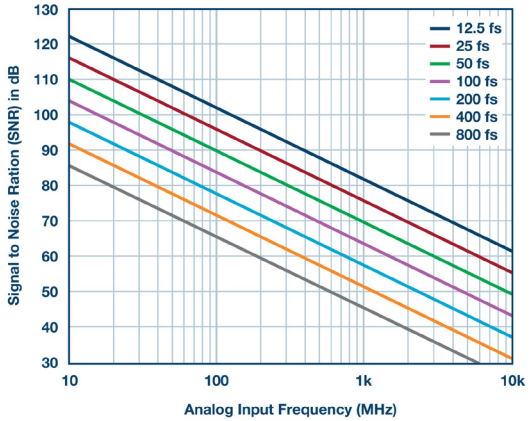
SHINE

ADC Performance

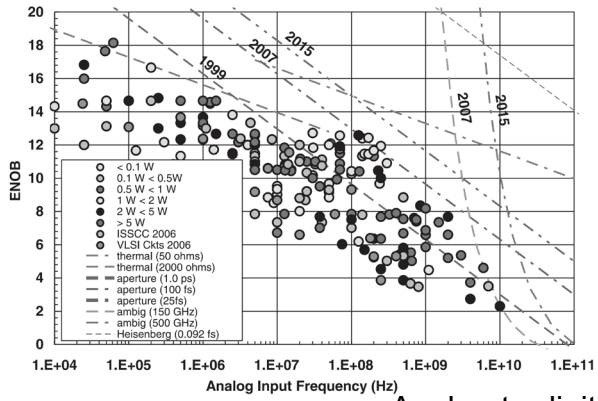
- SNR degrades with input frequency(fA) due only to aperture jitter(t_J)

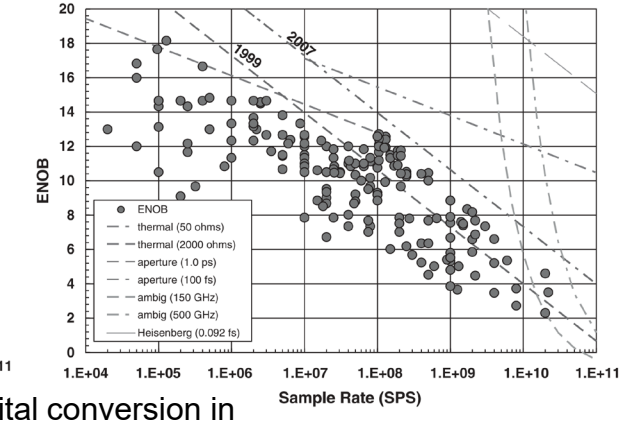
$$SNR = 20 \times log_{10}[1/(2 \times \pi \times fA \times t_J)]$$





Ramon Gomez, Senior Member, IEEE, Theoretical Comparison of Direct-Sampling Versus Heterodyne RF Receivers Noise Spectral Density: A New ADC Metric?

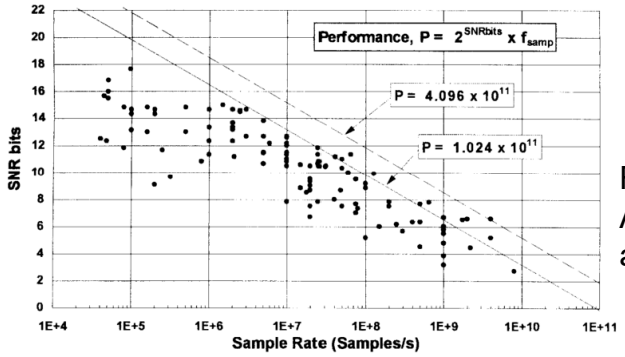




Analog-to-digital conversion in the early twenty-first century,

- ADC performance: $P = 2^{ENOB} \bullet f_s$

ADC1:ENOB=12, f_s=119MHz = **ADC2: ENOB=8, f_s=119*16MHz=1904MHz**

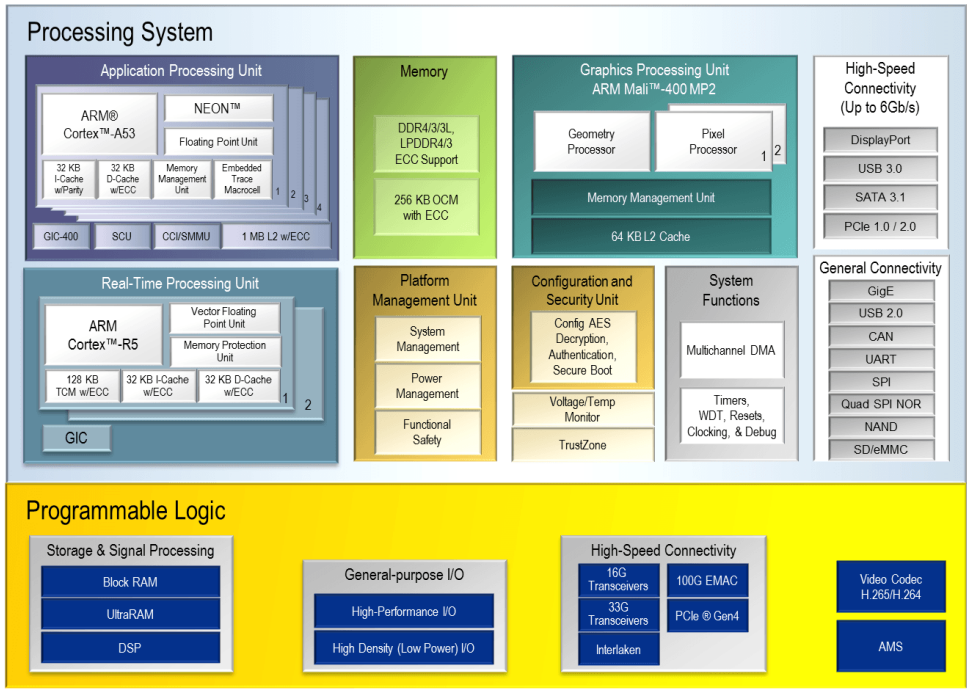


Robert H. Walden, Member, IEEE, Analog-to-digital converter survey and analysis

SHINE

SoC FPGA

- SoC FPGA with hard core ARMs and large logic resource simplify the electronic
- Supports high band width data transmission and complicate digital signal processing algorithms



Zynq UltraScale+ MPSoC FPGA

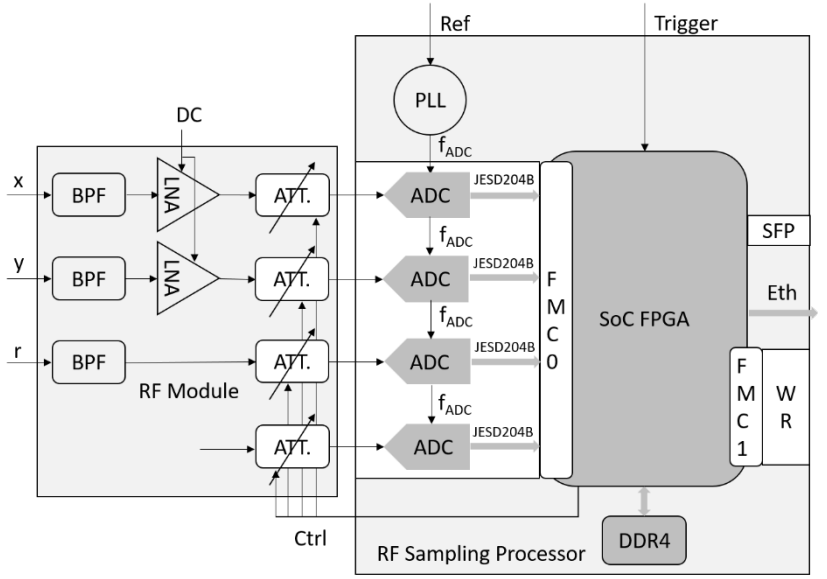
	Virtex5	ZU15EG	Promotion
ARM	0	4×Cortex-A53	New
LUT	28800	341280	×11.85
FF	28800	682560	×23.70
DRAM	480Kb	11.3Mb	×23.50
BRAM	2160Kb	26.2Mb	×12.13
DSP	48	3528	×73.5
UBRAM	0	31.5Mb	New
GTH	12×6.6Gb/s	24×16.3Gb/s	×4.94

RFDE Design for SHINE

- An SoC FPGA based RF direct sampling processor has been developed
- A RFDE for SHINE cavity BPM can be built with the processor

RF Direct Sampling Processor

Parameters	value
Channels	4
ADC bits	14
Bandwidth	9GHz
Max ADC rate	2.6GSPS
FPGA	Xilinx ZCU15EG
Clock	Ext./Int.
PL DDR4	2GB
Trigger	Ext./Self/Period
Interlock	Lemo
SFP	×4, UDP&Aurora
User GPIO	12
Software	Linux/EPICS



Block design of RFDE for SHINE Cavity BPM

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System Noise Figure

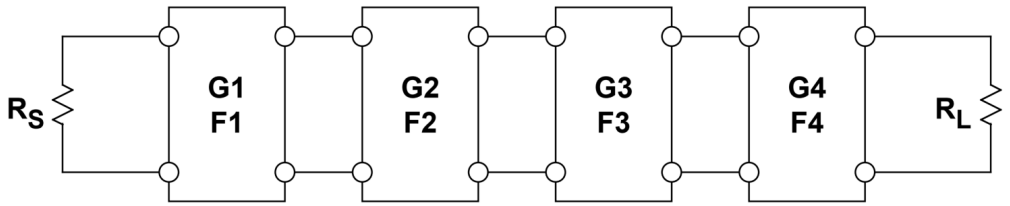
- Noise figure (NF) is defined as the ratio of signal-to-noise ratio (SNR) at the input to the SNR at the output

Noise factor: $F = \frac{S_i / N_i}{S_o / N_o}$ Noise figure: $NF = 10 * \log_{10}(F)$

- NF is used to characterize the noise of RF amplifiers, mixers, etc., it's a measure of the noise added by the device(degradation of the SNR from input to output).

$$NF = SNR_{i_{dB}} - SNR_{o_{dB}}$$

- NF of cascaded device chain



$$F_T = F1 + \frac{F2-1}{G1} + \frac{F3-1}{G1 \cdot G2} + \frac{F4-1}{G1 \cdot G2 \cdot G3} + \ldots$$

High gain in the first stage reduces the contribution of the NF of the second stage

NF of the first stage dominates the total NF

$$F = 10^{\frac{NF[dB]}{10}}$$

$$G = 10^{\frac{G[dB]}{10}}$$

SHINE

ADC Noise Figure

- For passive devices NF≈Insertion Loss, such as Mixer, Filter, Attenuator,
- ADC's NF calculation:

$$NF_{ADC} = P_{FULLSCAE}[dBm] - kTB - NSD_{ADC} =$$

$$P_{FULLSCAE}[dBm] + 174dBm - SNR_{ADC} - 10 \cdot \log\left(\frac{FS}{2}\right)$$

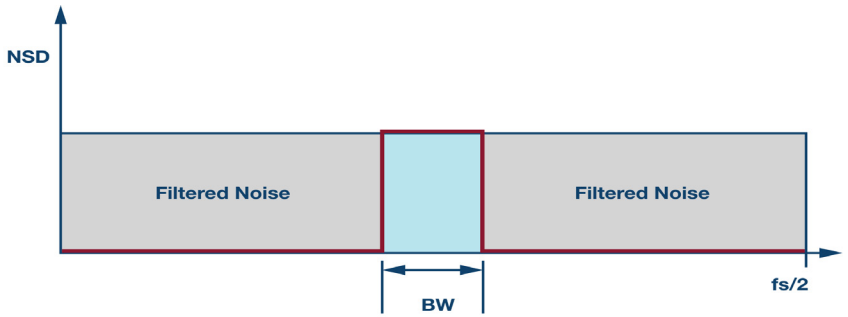
$$P_{FULLSCAE}[dBm] = 10 \cdot \log\left(1000 \cdot \frac{(Vpp)^2}{8 \cdot Z_{IN}}\right) \quad (4)$$

Tommy Neu, Direct RF conversion: From vision to reality, TI

	AD9265	ADC9680	ADC9689
Sampling rate(FS)	125M	1G	2.6G
Input full-scale (Vpp)	2V	1.7	1.7
Signal-to-noise ratio	79@70MHz	67.2@10MHz	58.3@3300MHz
Input impedance (Zin)	200	100	100
Calculated noise figure (dB)	21	25.4	30.1

Digital Signal Processing Gain

- Cavity BPM signal is narrow bandwidth(1.6MHz), much smaller than the Nyquist bandwidth(fs/2=1.3GHz)
- Digital signal processing to filter out the signal will produce processing gain



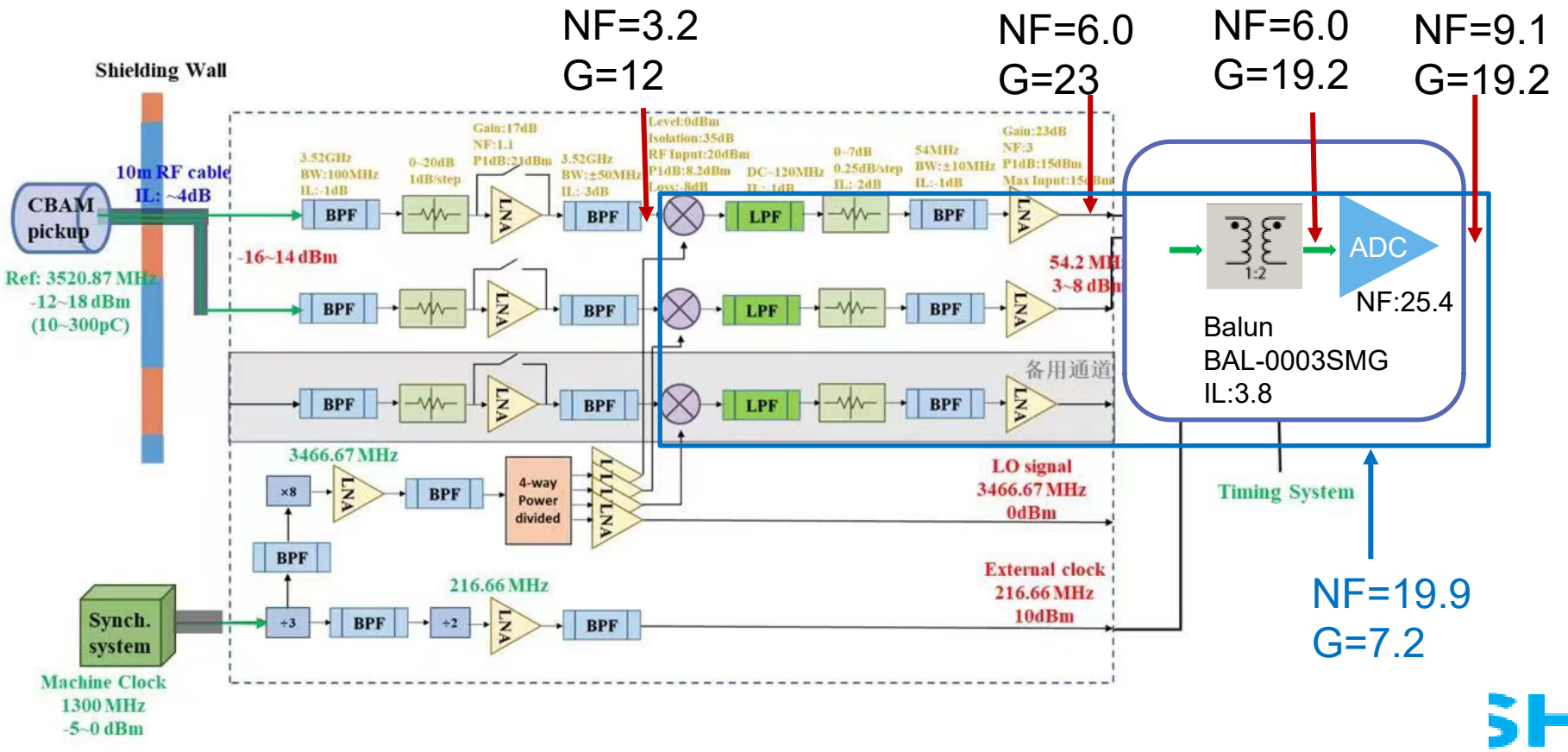
$$Processing\ gain = 10log_{10}(\mathrm{fs}/(2 \times BW))$$

IF processing gain: 10*log10(216.6*4/(2*1.6))=24.3dB

RFDE processing gain: 10*log10(216.6*12/(2*1.6))=29dB

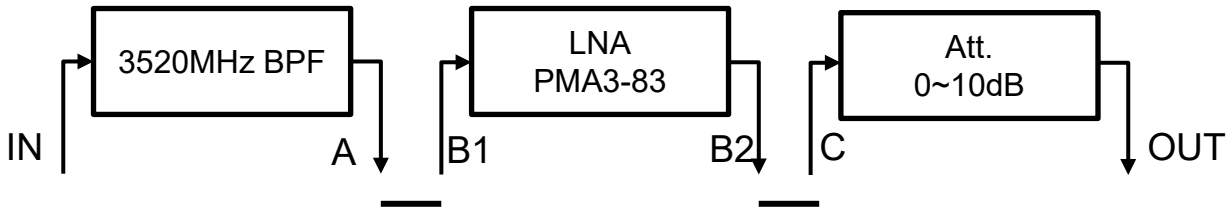
SHINE Heterodyne System Performance Analyzing

- SNR of SHINE cavity BPM signal is 72dB, the calculated NF is 9.1dB, add processing gain is 24.3dB, the SNR of the system is 72-9.1+24.3=87.2dB, the system relative error is 5×10^{-5}

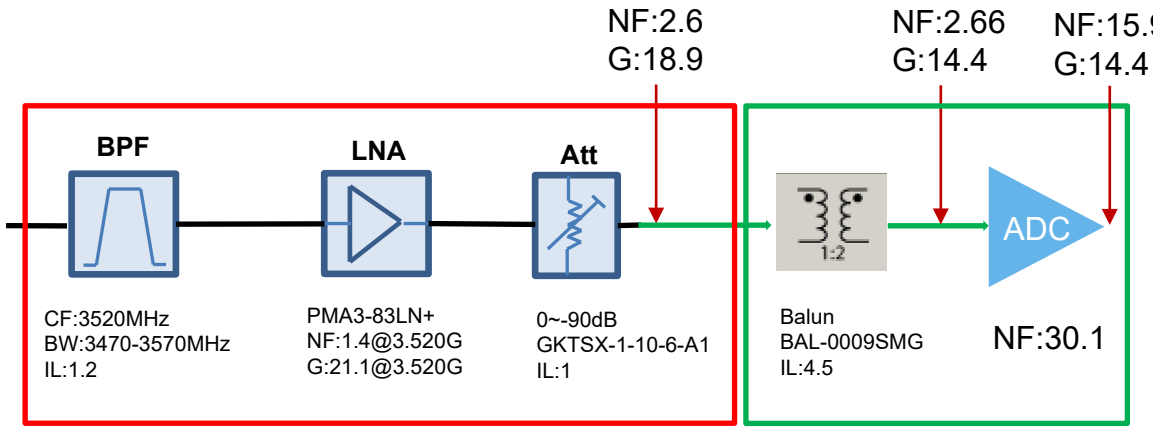


RFDE Performance Analyzing – A Prototype of RF Module

- A protype of RF module was built to evaluate the RFDE performance
- Assuming SNR of cavity BPM signal is 72dB, the calculated NF of DRFE is 15.9dB, add processing gain 29dB, the SNR of the system is 72-15.9+29=85dB, the ideal system relative error is 7×10^{-5}



Prototype of RF Module

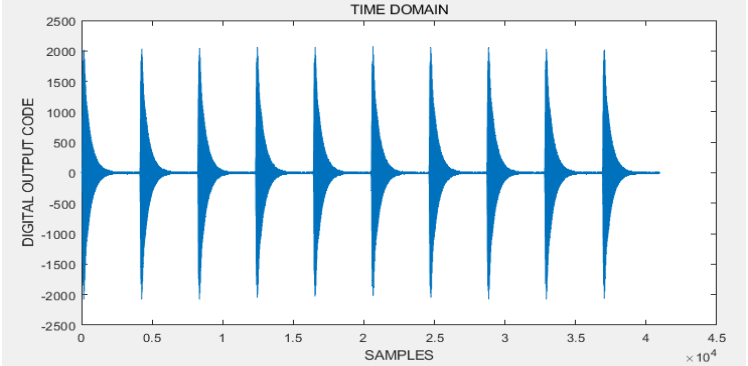


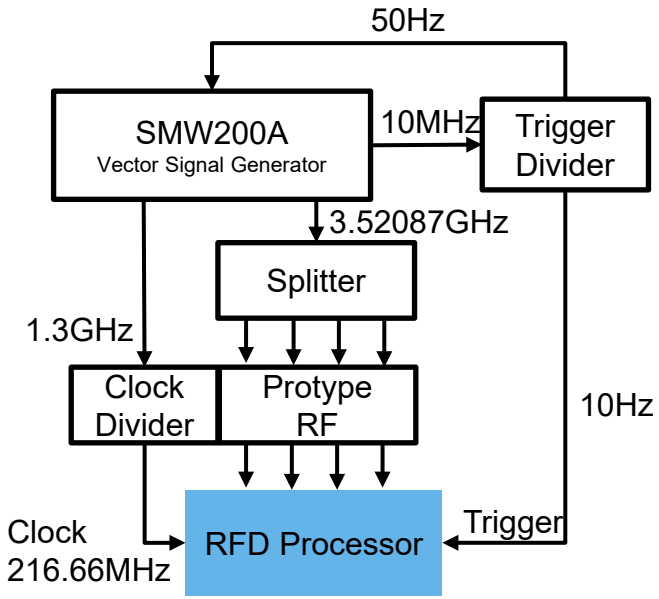
Prototype of RF Module

RFDE Performance Evaluation

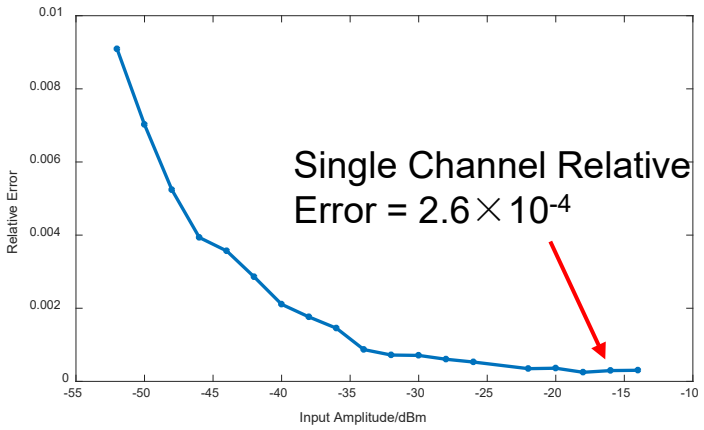
- A vector signal generator outputs phase locked decay RF signal(simulate cavity BPM signal) and clock signal
- Amplitude relative error of single channel is 3.0×10^{-4}
- Amplitude relative error between two channels is 2.0×10^{-4}

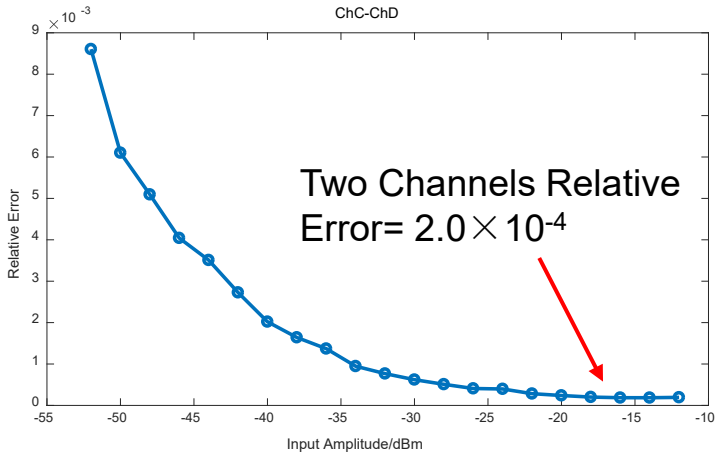
$< 1.0\times10^{-3}$





Lab test platform





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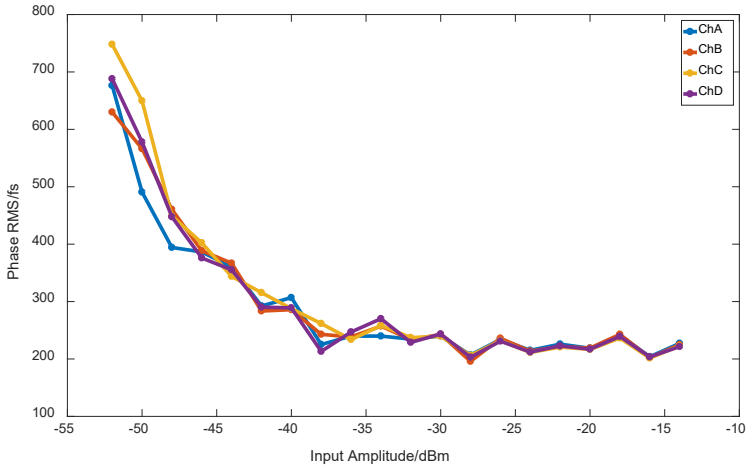
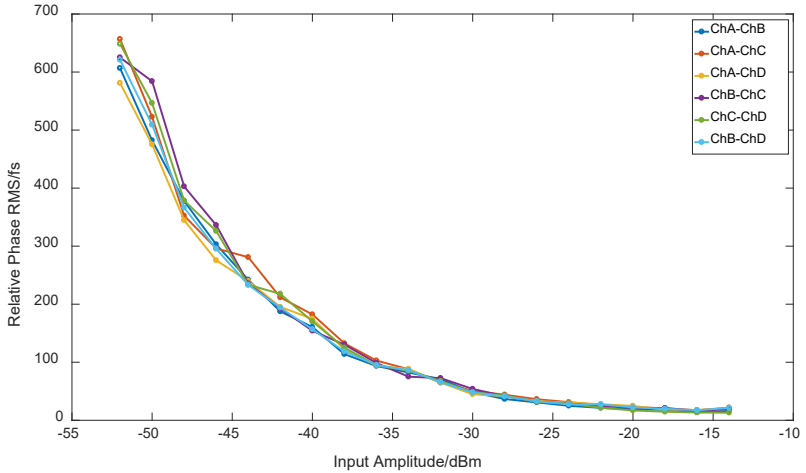
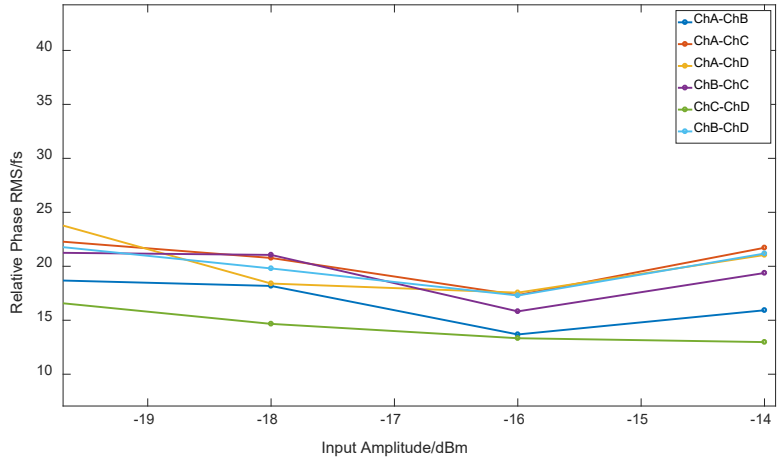
RFDE Performance Evaluation

- Single channel phase RMS 200fs(including jitter from signal source)
- Two channels relative phase RMS 14fs, better than 25fs CBAM requirement in SHINE

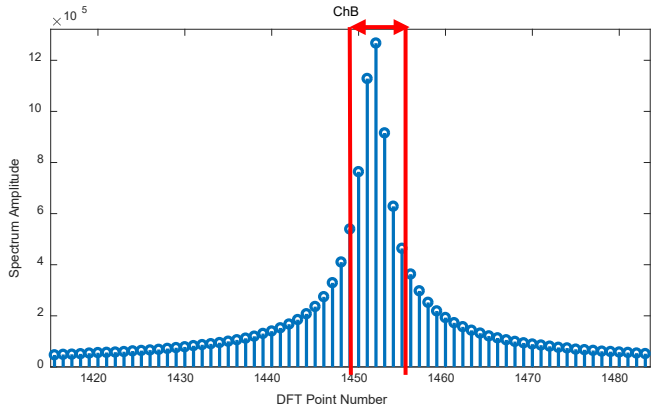


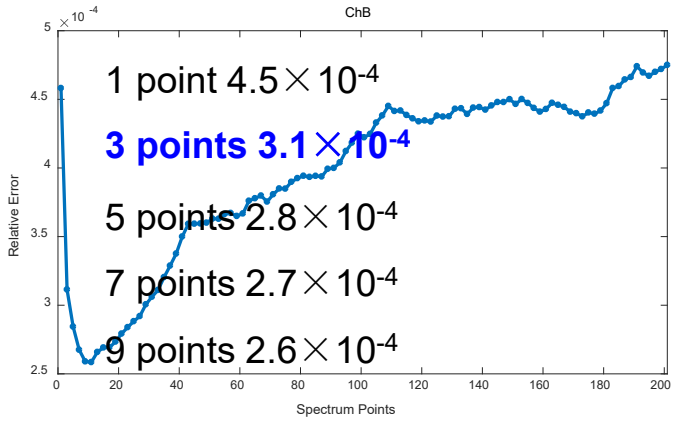




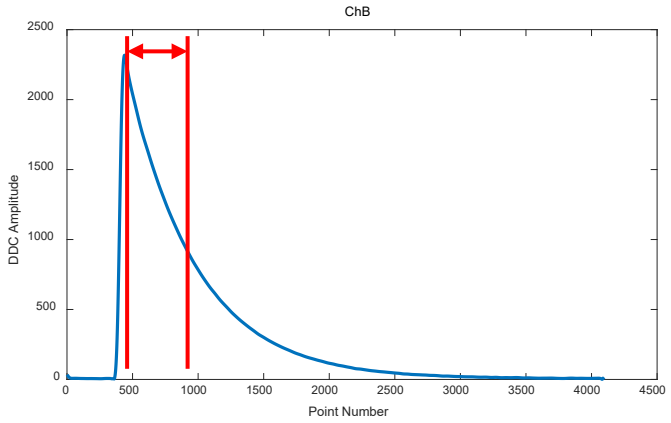
SHINE

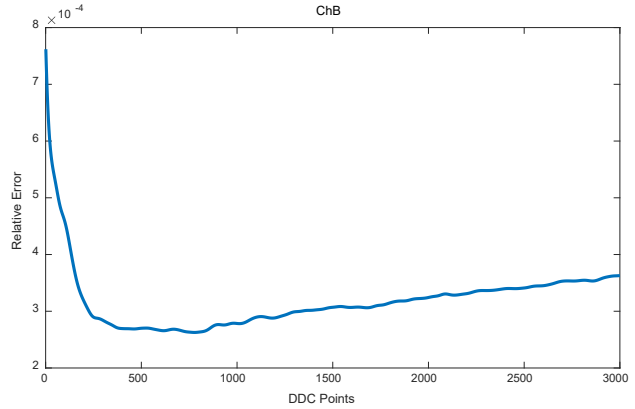
Digital Signal Processing Algorithms



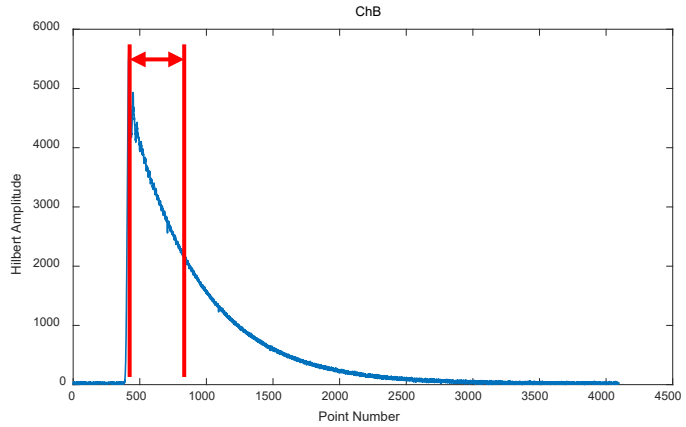


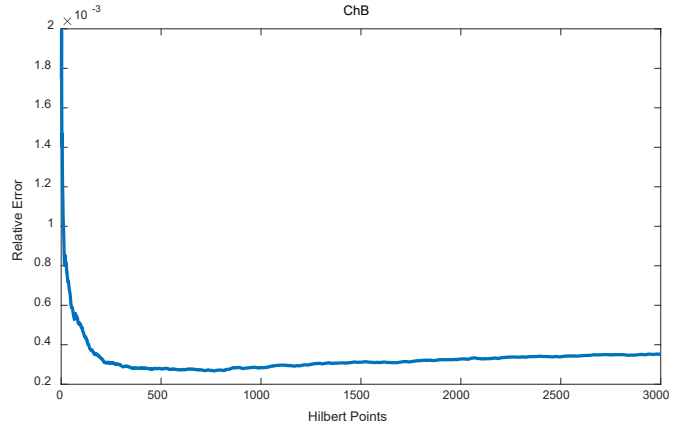
Goertzel-DFT algorithm





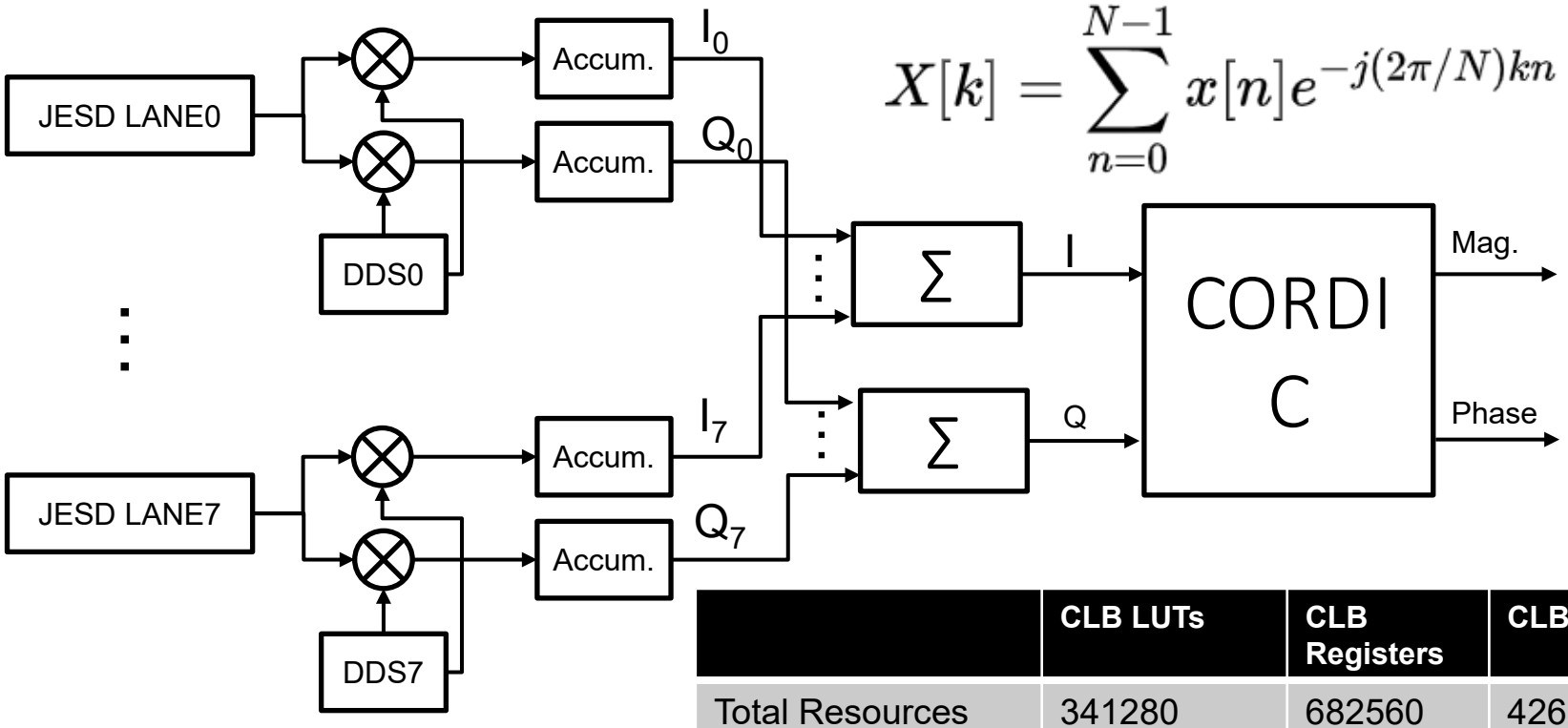
DDC algorithm





Hilbert algorithm

Goertzel-DFT FPGA Implementation



$$X[k] = \sum_{n=0}^{N-1} x[n] e^{-j(2\pi/N)kn} \quad , \text{其中} (0 \le k \le N-1)$$

	CLB LUTs	CLB Registers	CLB	LUT as Logic	LUT as Memory	Block Ram Tile	DSP
Total Resources	341280	682560	42660	341280	184320	744	3528
1 Point DFT CBPM Position Cost	28294	37778	4893	25633	2661	76.5	88
Percent	8.29%	5.53%	11.47%	7.51%	1.44%	10.28%	2.49%
Percent(3points)	24.9%	16.5%	34.5%	22.5%	4.5%	30.9%	7.5%

Is it time to use the RFDE in large-scale?

- Electronic technology is developing rapidly. Higher performance ICs(ADC, FPGA, PLL, DDR) are becoming more common. Budgets of electronics that were ten years ago can now build much higher performance electronics.
- RF Direct Sampling ADCs are more expensive than IF ADCs. But it is still cheaper compared to the cost savings from heterodyne RF modules.
- Yes, it's time to promote large-scale application of RFDE in beam diagnostics.

SSRF/SXFEL/DCLS Processor
Fs=125MHz，BW=650MHz

SSRF/SXFEL/DCLS SoC Processor
Fs=125MHz，BW=650MHz

SHINE Generic Processor
Fs=1GHz，BW=2GHz

RF Direct Sampling Processor
Fs=2.6GHz，BW=9GHz

SHINE

Thanks for your listening!