

LCLS-II Timing System and synchronous bunch data acquisition

TH1101

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14th September 2023

Agenda

LCLS-II Timing System and synchronous bunch data acquisition

Beamline MAP

LCLS-II Timing System, DESIGN:

- Timing Requirements
- Timing Distribution
- Timing Pattern Frame (individual pulse)

Timing Pattern Requirements

Beam Synchronous Acquisition services

- Beam Synchronous Acquisition (BSA)
- Beam Synchronous Scalar System (BSSS)

Timing Pattern Generator Graphical User Interface (TPGGUI)

- Patterns Classification

Timing Pattern Receivers

Commissioning Experience

SLAC Accelerator Complex: LCLS/CLTS/LCLS-II

Beam Line Map of the two timing systems serving LCLS and LCLS-II



LCLS-II will add a superconducting accelerator, occupying one-third of SLAC's original 2-mile-long linear accelerator tunnel.

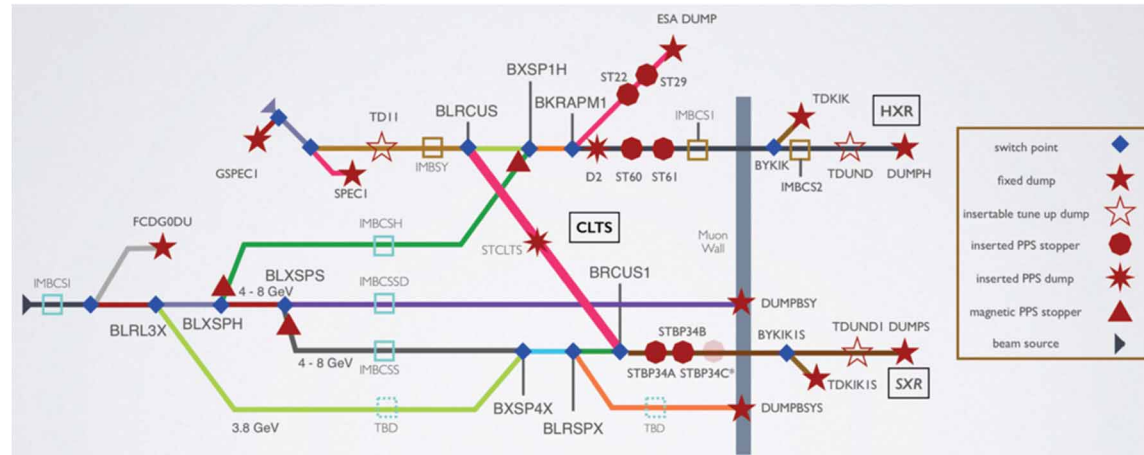
LCLS-II will provide a major jump in capability – moving from 120 pulses per second to 1 million pulses per second.

In addition to the new accelerator, LCLS-II requires a number of other cutting-edge components, including a new electron source, a powerful cooling plant that produces refrigerant for the accelerator, and new undulators to generate X-rays.

SLAC Accelerator Complex: LCLS/CLTS/LCLS-II

Beam Line Map of the two timing systems serving LCLS and LCLS-II

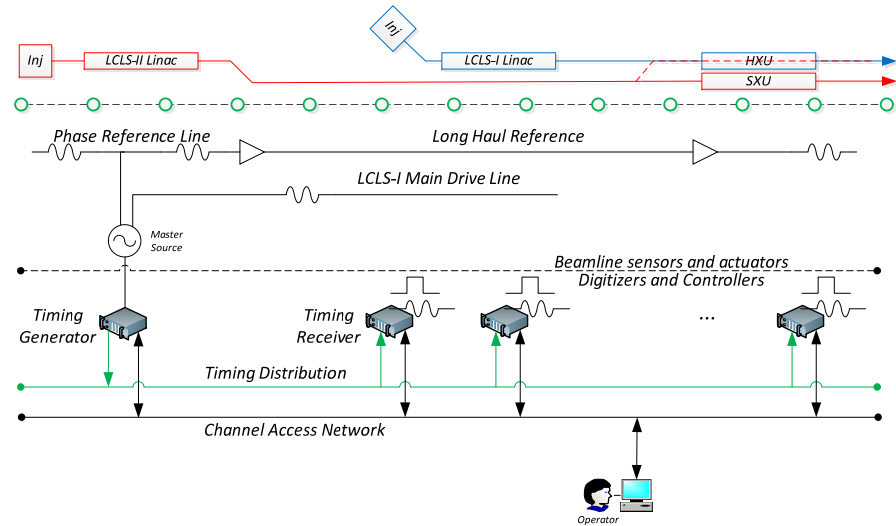
Map of LCLS / CLTS / LCLS-II highlighting the kickers and dumps



LCLS-II TIMING SYSTEM

DESIGN: REQUIREMENTS

Timing Attribute	Value
Phase Reference (Linac RF)	1300 MHz
Clock (Gun RF = Linac RF/7)	185.71 MHz
Nominal Beam Rate (Clock/200)	0.92857 MHz
Fiducial Resync Freq (Clock/2600)	0.07143 MHz
Fiducial (Power Line Phase)	360 Hz
Stability - Standard (fiber)	0.4 ns
Stability – Phase reference line (PRL)	1 fs/sec, 1 ps/day
Jitter – Standard (fiber)	30 ps
Jitter – PRL (50Hz to 5kHz)	0.005 ^σ or 10.7 fs



LCLS-II TIMING SYSTEM

Timing Pattern Receivers

Every control system crate has a timing receiver.

The hardware is ATCA or PCIe platform.

Timing Pattern is analyzed based on modules: tprTrigger, bsaDriver and other libraries.

The devices are triggered (total 16 configurable triggers) based on the appropriate filters for the given location, defined in one of the 16 channels.



SPD TPR Diagnostics Display - PyDM

File View History Tools

Tpr Diagnostics

TPR Name: TPR-SFD-MP04-0 Timing Uptime (sec): 3772360

Fiducial Counter: -1188701972 Timing Link Status: LINK Up

Mode: SC

SC: SC Expt SC Trig

NC: NC Expt NC Trig

Trigger Num	Desc	Tri Enable	TWID	TDES	Source	AND/OR	Pair Source	Rate
0	NC Kicker Abort	Disabled	0	0.00	Channel 00	Disable	TRG01	0.0
1	NC Kicker Standby	Disabled	0	0.00	Channel 00	Disable	TRG00	0.0
2	NC Kicker User Abort	Disabled	0	0.00	Channel 02	Disable	TRG03	0.0
3	Fire Signal Generator (not used)	Disabled	0	0.00	Channel 03	Disable	TRG02	3.0
4	Bunch Present (NC Only)	Enabled	0	0.00	Channel 04	Disable	TRG05	0.0
5	NC BSA Stream (NC Only)	Enabled	0	0.00	Channel 05	Disable	TRG04	0.0
6	AMC0 Waveform Stream	Enabled	0	0.00	Channel 06	Disable	TRG07	1.0
7	AMC1 Waveform Stream	Enabled	0	0.00	Channel 06	Disable	TRG06	2.0
8	Front Panel Trigger (TrigOut) Bay 0	Enabled	0	0.00	Channel 08	Disable	TRG09	1.0
9	Front Panel Trigger (TrigOut) Bay 1	Enabled	0	0.00	Channel 09	Disable	TRG08	1.0
10	ADC 0 Coarse Window	Enabled	0	0.00	Channel 10	Disable	TRG11	930000.0
11	ADC 1 Coarse Window	Enabled	0	0.00	Channel 10	Disable	TRG10	930000.0
12	ADC 2 Coarse Window	Enabled	0	0.00	Channel 10	Disable	TRG13	930000.0
13	ADC 3 Coarse Window	Enabled	0	0.00	Channel 10	Disable	TRG12	930000.0
14	ADC 4 Coarse Window	Enabled	0	0.00	Channel 10	Disable	TRG15	930000.0
15	ADC 5 Coarse Window	Enabled	0	0.00	Channel 10	Disable	TRG14	930000.0

SPD TPR SC Expert Display - PyDM

File View History Tools

Tpr Diagnostics

TPR Name: TPR-SFD-MP04-0 Timing Uptime (sec): 3772365

Fiducial Counter: 1605705873 Timing Link Status: LINK Up

Mode: SC

Device System Information

LCLS2 master delay (nsec): 127602

Ch #	Rate Mode	Fixed Rate	AC Rate	Timeslot Mask	Ctrl Seq Eng	Ctrl Seq Bit	Rate	Dest Mode	Dest Mask	Ch Enable	Event Counts
00	Fixed	1Hz	0.5Hz	TimeSlot	0	0	0.0	Inclusive	DestMask	0	0
01	Fixed	1Hz	0.5Hz	TimeSlot	0	0	0.0	Inclusive	DestMask	0	0
02	Fixed	1Hz	0.5Hz	TimeSlot	0	0	0.0	Inclusive	DestMask	0	0
03	Fixed	1Hz	0.5Hz	TimeSlot	0	0	1.0	Don't care	DestMask	0	584000.0
04	Fixed	1Hz	0.5Hz	TimeSlot	0	0	0.0	Inclusive	DestMask	0	0
05	Fixed	1Hz	0.5Hz	TimeSlot	0	0	0.0	Inclusive	DestMask	0	0
06	Fixed	1Hz	0.5Hz	TimeSlot	0	0	1.0	Don't care	DestMask	0	384000.0
07	Fixed	1Hz	0.5Hz	TimeSlot	0	0	0.0	Inclusive	DestMask	0	0
08	Fixed	1Hz	0.5Hz	TimeSlot	0	0	1.0	Don't care	DestMask	0	584000.0
09	Fixed	1Hz	0.5Hz	TimeSlot	0	0	1.0	Don't care	DestMask	0	384000.0
10	Fixed	1MHz	0.5Hz	TimeSlot	0	0	930000.0	Don't care	DestMask	0	377700000.0
11	Fixed	1Hz	0.5Hz	TimeSlot	0	0	0.0	Inclusive	DestMask	0	0
12	Fixed	1Hz	0.5Hz	TimeSlot	0	0	0.0	Inclusive	DestMask	0	0
13	Fixed	1Hz	0.5Hz	TimeSlot	0	0	0.0	Inclusive	DestMask	0	0
14	Fixed	1Hz	0.5Hz	TimeSlot	0	0	0.0	Inclusive	DestMask	0	0
15	Fixed	1Hz	0.5Hz	TimeSlot	0	0	0.0	Inclusive	DestMask	0	0

LCLS-II TIMING SYSTEM

DESIGN: REQUIREMENTS

AC Rate compatibility for some of the devices, like Klystrons (XTCAV and STCAV). The triggering system for these devices needs to be synchronized to the AC Power line timeslots and up to a max 120Hz.

The requirement of the diagnostics devices along the machine is to take clean measurements. Since the performance of the above listed devices depends on the triggers being synchronized to the AC power line phase. If this isn't aligned the Klystron impulse will have a jitter in amplitude, not producing a clean measurement.

An example is in the Diagnostic Line destination, just after the gun where we'll expect to trigger on AC patterns limited to 120Hz.

The TCAV diagnostics provide a transverse kick of the electron beam. Their triggers must be aligned to the AC power line to minimize jitter.

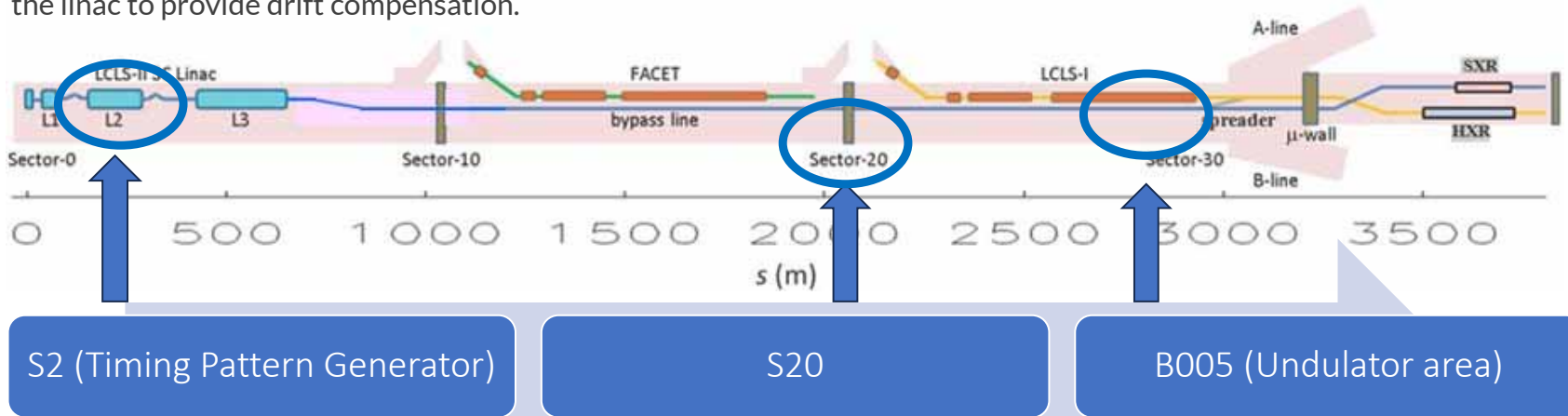
LCLS-II TIMING SYSTEM

DESIGN: TIMING DISTRIBUTION

LCLS-II Timing System is completely decoupled from LCLS-I Timing System.

Timing Pattern Generator (TPG) sends Timing Frames to each Timing Pattern Receiver (TPR) over a dedicated fiber network at 1MHz.

Challenge: signal stability over this long fiber network. Active Fanout devices operate at three strategic locations along the linac to provide drift compensation.



LCLS-II TIMING SYSTEM

DESIGN: TIMING DISTRIBUTION

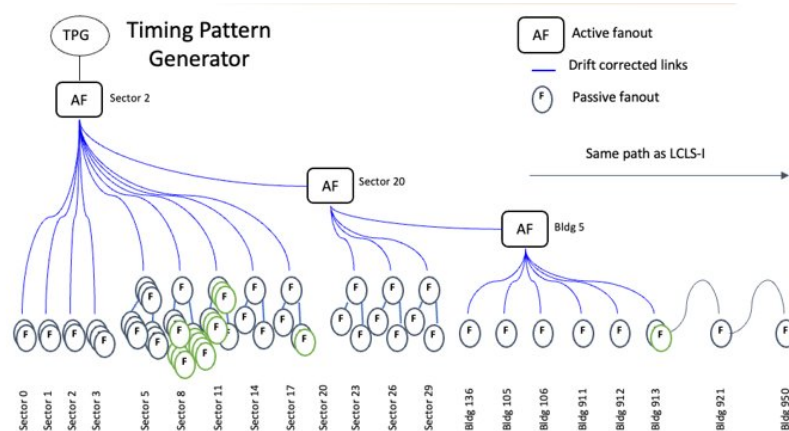
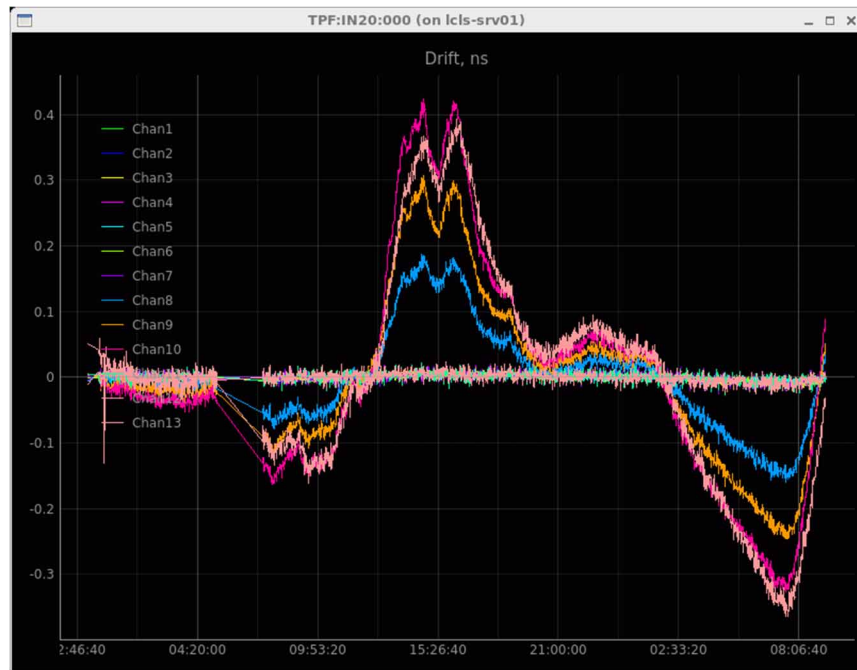


Figure shows the drift over 6 channels in S20 due to length and heat load.

LCLS-II TIMING SYSTEM

DESIGN: TIMING FRAME (at glance)

- Timestamp
- PulseID -> Label each pulse with global pulseID for correlation across devices
- Destination -> destination tag for each pulse
- Fixed Rates -> Fixed Rate Markers 0-9 one bit each computed by dividing 186MHz refclk by one of 1,13,91, 910, 9100, 91000
- AC Rates -> Power Line Synchronized markers (req. option to sync to power line)
- Beam Request -> Beam is requested by Inj gun
- Requested Charge [pC]
- Machine Protection System (MPS) Valid
- Beam Containment System (BCS) Fault
- MPS Limiting
- MPS Limits
- Beam Synchronous Acquisition (BSA) fields (Init; Active: AvgDone; Update) *
- Sequence Control Bits 288

**This will be explained in the next few slides*

The timing pattern consists of a sequence of timing frames, which contains data set by firmware and software.

LCLS-II TIMING SYSTEM

Timing Pattern Requirements

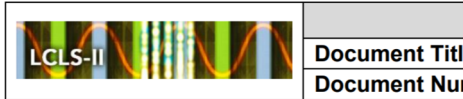
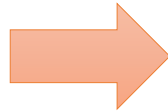


Table 2: A list of beam allowable rates increase nominally 1 Hz.

Nominal rate	Exact rate
Zero rate	0
Single shot	<ul style="list-style-type: none"> Once, on req
Burst mode	<ul style="list-style-type: none"> Specify number Specify spacing
1 Hz	0.928 Hz
10 Hz	9.28 Hz
50 Hz	46.4 Hz
100 Hz	92.8 Hz
1 kHz	0.928 kHz
10 kHz	9.28 kHz
100 kHz	92.8 kHz
Half rate	464.285 kHz
Full rate	928.571 kHz



FIXED RATE Patterns	Burst Spacing	Burst bunch(es)
0Hz	2-20	100
Single shot	9	2;5;10;20;50;100
1Hz	1,2	1;2-
10Hz		21;50;100;200;500;1000;2000
50Hz	10000	2
100Hz		
1KHz		
10KHz		
100KHz		
496KHz		
930KHz		
AC RATE Patterns		
0Hz		
1Hz		
10Hz		
30Hz		
60Hz		
110Hz		
119Hz		
120Hz		

LCLS-II TIMING SYSTEM

Timing Pattern Requirements

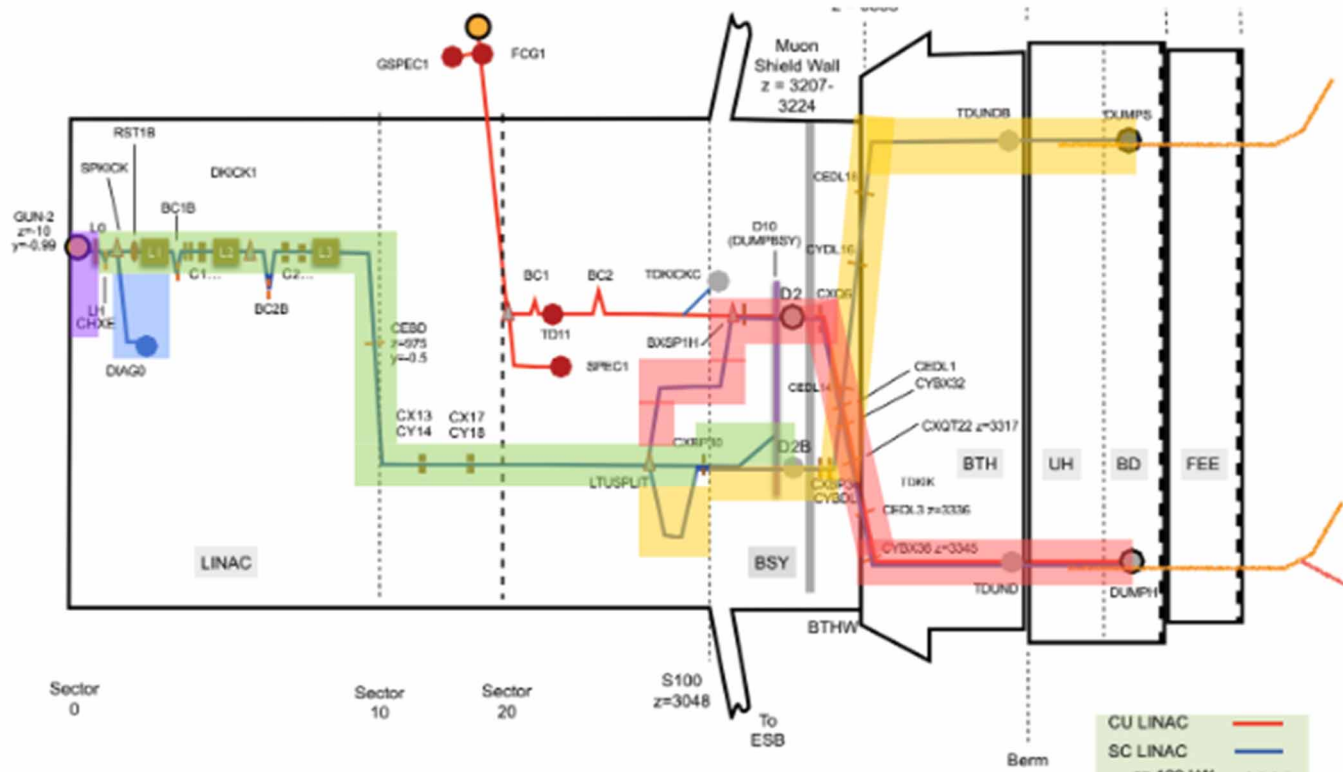
Timing Pattern Generator has 3 main types of Engines on FPGA:

- Beam Engines: Schedule beam patterns
- Allow Engines: Handshake MPS/Timing
 - Allow table – agreement on (spacing between pulses with beam, charge and window to evaluate the pattern)
- Experimental/Control Engines: Controls bits to support multi-destination beam, beam synchronous acquisitions, experiments requirements...

The screenshot shows the LCLS Home - PyDM interface. The 'SC TIMING PATTERN SELECTION' section is active, showing 'Mode: SC18'. Under 'Continuous Pattern Select', 'Continuous' is selected. The 'Rate Mode' is 'Fixed'. The 'Destination' is 'SC_DIAG0'. The 'Frequency' is '0Hz'. The 'Bunch Charge Set Point' is '50 pC'. The 'Selected Frequency' row shows '0Hz', '0Hz', '0Hz', and '1Hz'. The 'Bunch Charge Set Point' row shows '50 pC'. The 'Select' section shows 'Destination: SC_DIAG0 SC_BSYD SC_HXR SC_SXR'. The 'Pattern (bunches*)' row shows '- - - -'. The 'Sp. (bunches)' row shows '0 0 4 1'. The 'Pattern (spaces*)' row shows '- - - -'. The 'Selected Spaces' row shows '4 1 1 1'. The 'Bunch Charge Set Point' row shows '50 pC'. The 'SC TIMING STATUS' section is also visible, showing a table of parameters.

SC TIMING STATUS						
Destination: LASER ONLY	SC_DIAG0	SC_BSYD	SC_HXR	SC_SXR	SC_DASEL	
Request Rate: 0	0	0	0	10	0	
Actual Rate: 0	0	0	0	10	0	
MPS Beam Class RBV: Unlimited	Beam Off	Diagnostic	Beam Off	BC10Hz	Beam Off	
Timing Beam Class set PV: Diagnostic	BC120Hz	BC10Hz	BC10Hz	BC10Hz	Kicker STBY	
Timing Beam Class RBV: Beam Off	Beam Off	BC10Hz	Beam Off	BC10Hz	Beam Off	
Loaded Pattern: 0 Hz	0 Hz	0 Hz	0 Hz	10 Hz	0 Hz	
Charge Set Point RBV: 50	nC					

LCLS-II TIMING SYSTEM



LCLS-II TIMING SYSTEM

Timing Pattern Requirements – Compatibility lookup table

Mode		SC10	SC11	SC12	SC13	SC14	SC15	SC16	SC17	SC18	SC19	Type Patterns MPS Allowed
	Destination Per modes	SC1 Laser	SC1 Gun	SC1 TDINJ	SC1 DIAG0	SC1 DumpBSY	SC1 TDUNDHXR	SC1 TDUNDSXR	SC1 DUMPHXR	SC1 DUMPSXR	SC1 S30XL	
SC10	SC1 Laser	-										Override All
SC11	SC1 Gun		-									Screen limit 10Hz
SC12	SC1 TDINJ			-								Full rate and charge
SC13	SC1 DIAG0				-							AC Rates up to 120Hz
SC14	SC1 DumpBSY				Comp, Interl.	-						Full power but below 120KW
SC15	SC1 TDUNDHXR				Comp, Interl.	Comp, Interl.	-					10Hz
SC16	SC1 TDUNDSXR				Comp, Interl.	Comp, Interl.	Comp, Interl.	-				10Hz
SC17	SC1 DUMPHXR				Comp, Interl.	Comp, Interl.	Comp, Interl.	Comp, Interl.	-			Full rate
SC18	SC1 DUMPSXR				Comp, Interl.	Comp, Interl.	Comp, Interl.	Comp, Interl.	Comp, Interl.	-		Full rate
SC19	SC1 S30XL				Comp, Interl.	Comp, Interl.	Comp, Interl.	Comp, Interl.	Comp, Interl.	Comp, Interl.	-	Special case has 3 modes

LCLS-II TIMING SYSTEM

BEAM SYNCHRONOUS DATA SERVICES

This is a Single Pulse machine: The data acquisition requirement is to have all devices acquiring on the same bunch

SC BSA provides data buffers time stamped by the SC Timing System (Timing Pattern Generator – TPG).

SC BSA provides data filtering according to user needs.

SC BSA provides data buffers:

Maximum of 20000 data points.

Each data point can be an average of up to 8000 beam pulses

Maximum rate up to 1MHz

Beam Synchronous Scaler Service (BSSS) provides pulse by pulse scalars up to 100Hz for control room displays

LCLS-II TIMING SYSTEM

BEAM SYNCHRONOUS DATA SERVICES

- 29 User Defined Buffers

- 15 SYS Buffers 

Example:

SCD1H =

SC -> Super Conducting

D -> Diag0

1H -> 1Hz

1H is for the archive

TH is for displays

HH is for physics apps

System BSA Buffer	Beam Destination(s)	Beam Rate to beam destination(s)
<i>SCD1H</i>	D= <i>Diag0</i>	1 Hz
<i>SCDTH</i>	D= <i>Diag0</i>	10 Hz
<i>SCDHH</i>	D= <i>Diag0</i>	100 Hz
<i>SCL1H</i>	L=LINAC (= SC_BSYP OR SC_HXR OR SC_SXR)	1 Hz
<i>SCLTH</i>	L=LINAC (= SC_BSYP OR SC_HXR OR SC_SXR)	10 Hz
<i>SCLHH</i>	L=LINAC (= SC_BSYP OR SC_HXR OR SC_SXR)	100 Hz
<i>SCB1H</i>	B= SC_BSYP	1 Hz
<i>SCBTH</i>	B= SC_BSYP	10 Hz
<i>SCBHH</i>	B= SC_BSYP	100 Hz
<i>SCH1H</i>	H= SC_HXR	1 Hz
<i>SCHTH</i>	H= SC_HXR	10 Hz
<i>SCHHH</i>	H= SC_HXR	100 Hz
<i>SCS1H</i>	S= SC_SXR	1 Hz
<i>SCSTH</i>	S= SC_SXR	10 Hz
<i>SCSHH</i>	S= SC_SXR	100 Hz

LCLS-II TIMING SYSTEM

Timing Pattern Generator

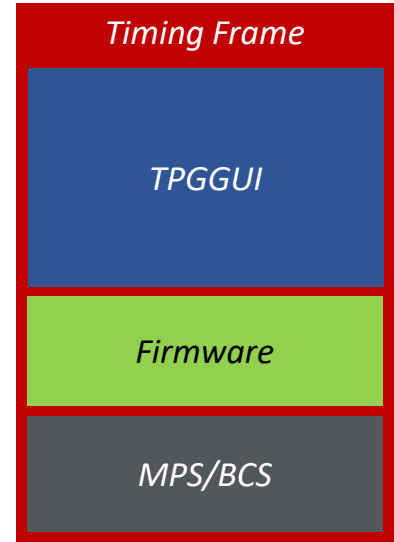
Patterns Classification:

- Standard Patterns: Single destination patterns for Fixed Rates, AC Rates and bursts.
- Complex Patterns:
 - Pulse Stealing: all pulses with beam land on the Fixed Rate Markers distributed as part of the timing pattern. In case of multiple destination requesting beam, destination priority assigns beam pulses
 - Interleaved Patterns: each destination is assigned an offset from the closest fixed rate marker to the requested beam rate. The subharmonic frequency that allows to lock the two LINAC (LCLS-I and LCLS-II) is 71.5KHz. Between two fixed rate pulses at 71.5KHz there are 13 empty pulses. The offset of empty pulses from a Fixed Rate marker, per destination, is then selected to be one of the prime numbers <13. Such as: 3 for DIAG0, 5 for HXR and 7 for SXR. This logic allows to resolve the beam request conflict when requesting beam to two destination.
 - Bunch Train: user defined interval between beam patterns (uses the patterns from the first and second bullet)

LCLS-II TIMING SYSTEM

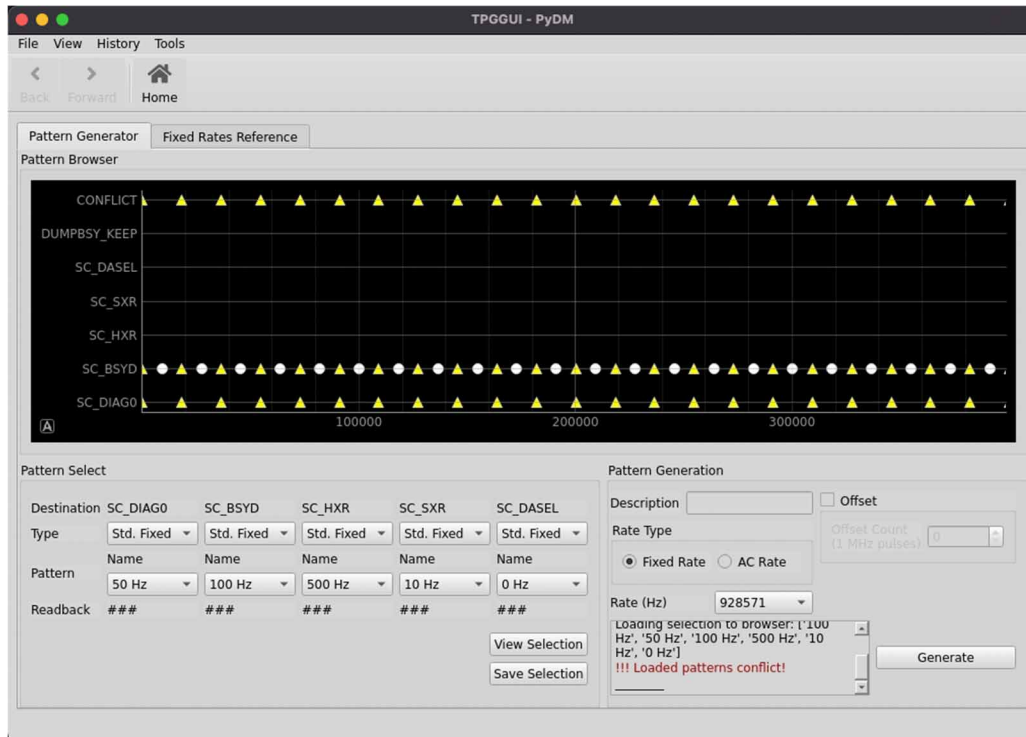
Timing Pattern Generator (TPG) Graphical User Interface (GUI)

- The timing system sends out a timing pattern that contains relevant information to trigger the LASER system to generate beam and to the timing clients and devices along the SC LINAC.
- The timing pattern consists of a sequence of timing frames, which contains data set by firmware and software.
- The firmware defines information that is constantly sent out to identify frames, such as rate specific markers, pulse ID. Other bits in the timing frame are machine operation sensitive and need to be configured at a higher level.
- The TPGGUI is the software tool used to program timing frames, updating information to the timing pattern to fulfill Operation requirements.
- The TPGGUI allows operations to program more complex patterns and schedule beam going to multiple destinations while meeting machine and personnel safety requirements.

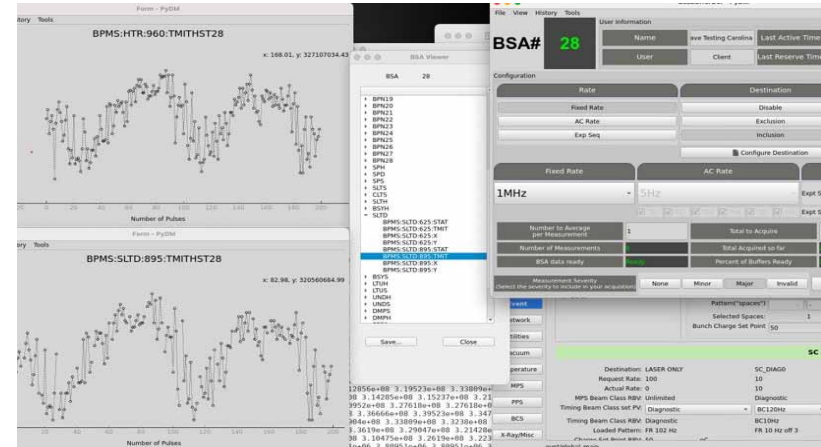
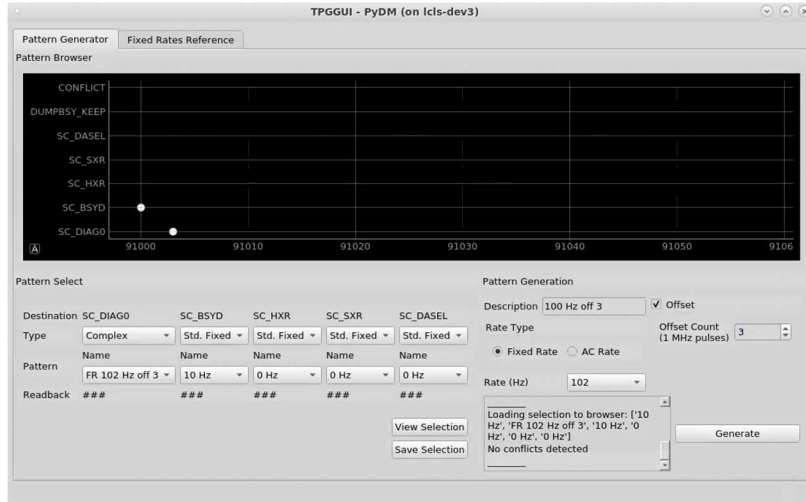


LCLS-II TIMING SYSTEM

Timing Pattern Generator Graphical User Interface (TPGGUI)



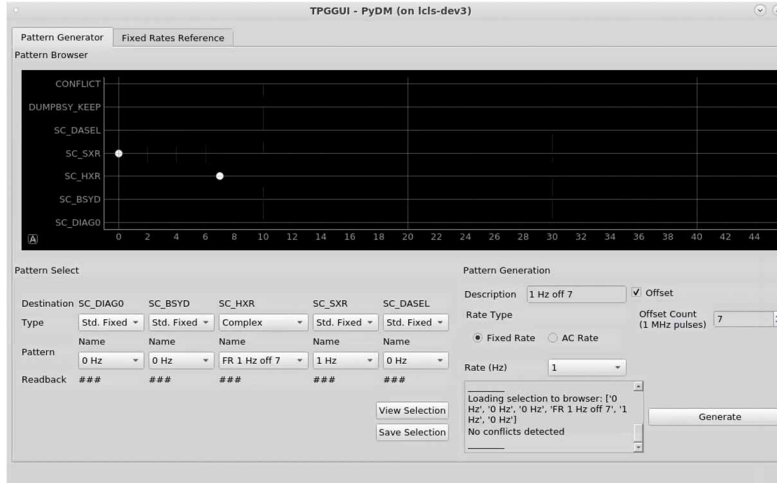
LCLS-II TIMING SYSTEM



Commissioning Experience: SC_DIAGO and SC_BSYD Interleaved

Not equally spaced pattern where beam is schedule to both destination in SC_DIAGO and SC_BSYD.
SC_DIAGO is off by 3 pulses from Fixed Rate Marker 100Hz.
Scheduled pattern will be 100Hz to DIAGO and 10Hz to BSYD with result to have 100Hz to DIAGO and 10Hz to BSYD.

LCLS-II TIMING SYSTEM

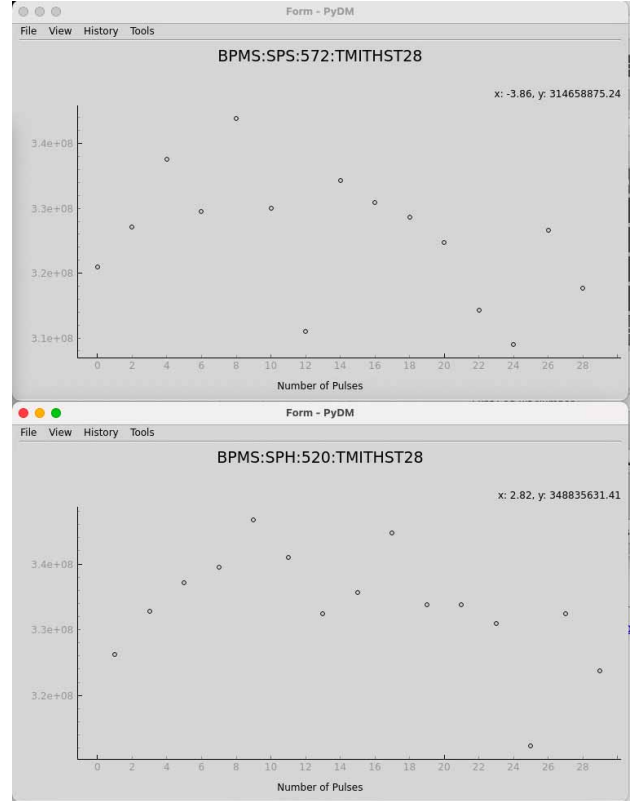


Commissioning Experience: SC_HXR and SC_SXR Interleaved

Not equally spaced pattern where beam is schedule to both destination in SC_HXR and SC_SXR.

SC_HXR here is off by 5 pulses from Fixed Rate Marker 1Hz and SC_SXR is on the mark.

Scheduled pattern will be 1Hz to SC_HXR and 1Hz to SC_SXR with result to have 1Hz to SC_HXR and 1Hz to SC_SXR.



Thank you

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