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BEAM INSTRUMENTATION HARDWARE ARCHITECTURE FOR UPGRADES AT THE BNL COLLIDER-ACCELERATOR COMPLEX AND THE FUTURE ELECTRON ION COLLIDER*

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Abstract

Many beam instrumentation systems at Brookhaven National Laboratory's Collider-Accelerator complex are over 20 years old and in need of upgrading due to obsolete components, old technology and the desire to provide improved performance and enhanced capabilities. In addition, many new beam instrumentation systems will be developed for the future Electron Ion Collider (EIC) that will be housed in the existing Relativistic Heavy Ion Collider (RHIC) tunnel. A new BNL designed custom hardware architecture is planned for both upgrades in the existing facility and new systems for the EIC. A general-purpose carrier board based on the Xilinx Zynq Ultrascale+ System-on-Chip (SoC) will interface with a family of application specific daughter cards to satisfy the requirements for each system. This paper will present the general architecture that is planned, as well as details for some of the application specific daughter cards that will be developed.

EXISTING FACILITY HARDWARE

When RHIC was commissioned in 2000, the majority of instrumentation systems were based on the VME platform. While this has worked very well over the years, options for system upgrades and new systems for the EIC have been carefully considered [1].

A custom-designed Beam Position Monitor (BPM) module (named V301) was developed in 2015 that uses the VME form factor but does not include a VME bus interface [2]. Each module instead includes a direct Ethernet communication interface for higher level control and general data transfer. The V301 is based on the Xilinx Zynq gate array. Four 400 MSPS ADC converters are provided for measurement of BPM pickup signals and onboard filter options are included to process electrons or ions with various bunch repetition rates. The on-board Zynq ARM processor runs Linux with embedded software for processing and communication to higher level systems. Beam synchronous clocks are received by a single board in the chassis and distributed via unused P2 pins to all of the V301 modules. One major benefit of this system is that up to 15 V301 boards can be housed in a single VME chassis, and module replacement is very simple when necessary.

Another VME form factor module (named V340) based on the Zynq Ultrascale+ SoC was also recently developed. This module includes a high pin count FMC connector to enable using both custom and 3rd party FMC modules. The V340 is planned to be used for current transformer data acquisition and processing, as well as other applications.

In 2009 the RHIC RF group developed a Xilinx Virtex-5 based carrier board with custom daughter cards specific for RF applications [3]. This system is housed in a custom developed 3U chassis and runs the VxWorks real-time operating system directly on the Virtex 5 gate array.

OVERVIEW OF THE EIC

The EIC is scheduled to be fully commissioned with beam in 2034 and consists of the following major subsystems as shown in Fig. 1:

- Existing Hadron injector systems
- Hadron Storage Ring (HSR)
- Electron Pre-Injector (Polarized electron source and Linac)
- Rapid Cycling Synchrotron (electron accelerator) (RCS)
- Electron Storage Ring (ESR)

The existing Collider-Accelerator complex injector systems - Tandem, Electron Beam Ion Source (EBIS), Linac with polarized proton source, booster and Alternating Gradient Synchrotron (AGS) - will continue to be used for injection into the new HSR. Therefore, the existing systems need to be maintained and/or upgraded to support the EIC operation. The HSR will reuse significant portions of the existing Relativistic Heavy Ion Collider (RHIC) machine which is scheduled to complete its final beam run in 2025. The electron pre-injector, RCS and ESR will be completely new machines.

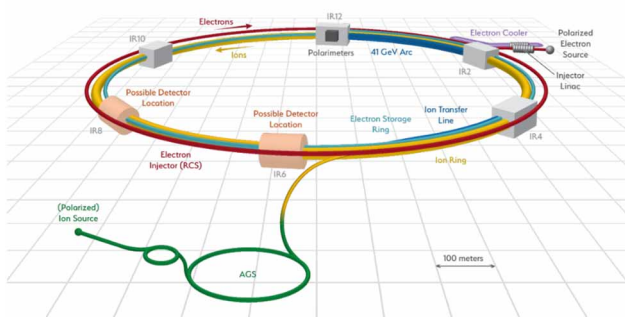

Figure 1: Layout of EIC.

Figure 2 lists the new instrumentation systems planned to be developed for the EIC machine. Note that this list does not include systems that are planned to be upgraded for the existing hadron injector systems.

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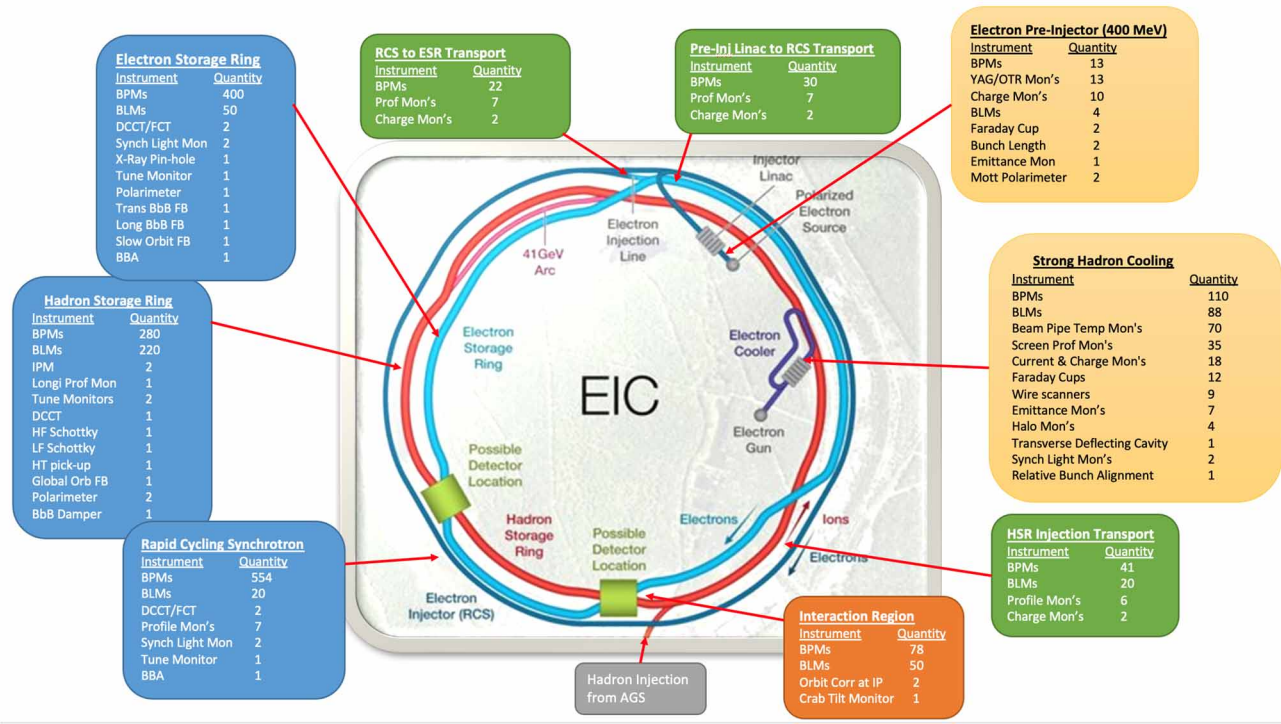

Figure 2: EIC instrumentation list for each subsystem, excluding the existing hadron injector machines.

OVERVIEW OF COMMON PLATFORM

The knowledge gained from the RF developed Virtex-5 based system, the Instrumentation System V301 Zynq-based BPM module and the V340 Ultrascale+ based module has been instrumental in the evolution to the new Xilinx Zynq Ultrascale+ SoC based carrier module that will accommodate 2 daughter cards via custom-defined pinouts on high-speed connectors. A mockup of the system is provided in Fig. 3.

Figure 3: Mockup of common platform chassis with carrier module and one of two daughter cards installed.

Carrier Module

A block diagram of the common platform carrier module is provided in Fig. 4. The external dimensions of the module are 15.5" wide by 10" deep, with a 3" x 6" cut-out for the power supply module.

The major features include:

- Xilinx Zynq Ultrascale+ SoC
- 4 GB DDR4 memory
- 4 120-pin connectors to support 2 daughter sites
- 8 SFP modules with crosspoint switch for configurable routing to on-board Ultrascale+ or daughter sites
- Dual RJ-45 Ethernet ports
- RJ-45 connector for RS-232 serial console port
- 16 Digital I/O LEMO connectors, 4 inputs, 4 outputs, 8 bidirectional
- External clock input passed to the daughter sites
- System clock input with PLL for generating beam synchronous clocks

Daughter Cards

A suite of daughter cards is in the process of being developed to support controls, RF, beam instrumentation and other applications.

Each daughter card will include a gate array for local control and for communication and data transfer to/from the carrier module. A memory mapped interface will be implemented between the carrier and daughter modules using AXI (Advanced eXtensible Interface) buses bridged by a Xilinx AXI Chip2Chip core over a Xilinx Aurora serial link. For large buffers of data, dedicated DDR memory may be provided on the daughter card and transferred to higher level workstations either by the carrier module after transferring the data from the daughter card to the carrier module memory or directly through a dedicated Ethernet connection on the daughter card.

The daughter cards slide into the front of the chassis with rails to guide the board to the carrier module connectors.

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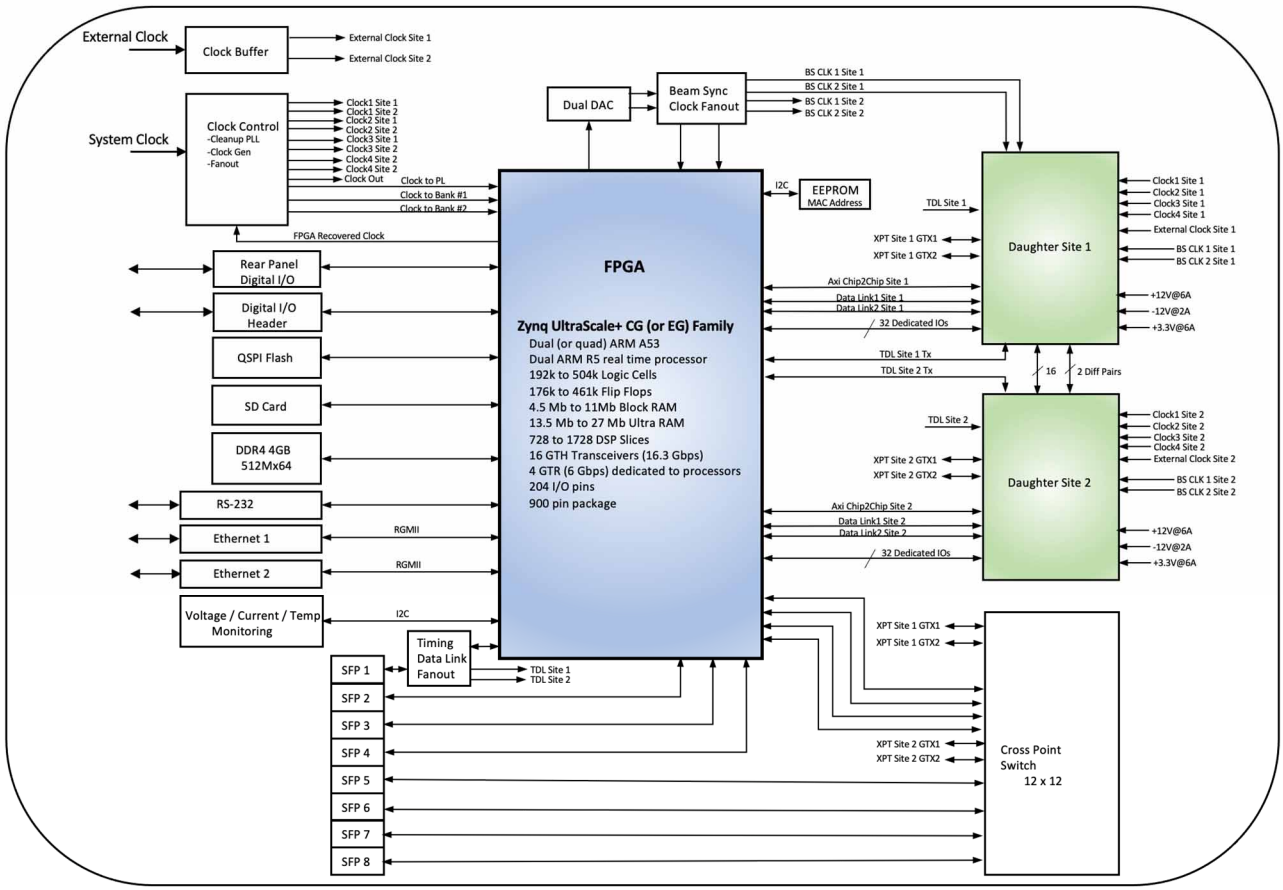

Figure 4: Block diagram of common platform carrier board.

The carrier module will provide +3.3 V@8 A, +12 V@6 A and -12 V@2 A to each daughter card. Two Samtec ERM8-060-01-L-D-EM2 connectors on each daughter card will be used for communication between the carrier module and the daughter card.

Signal Conditioner Modules

Some daughter cards will be designed to accommodate a signal conditioner module that can include buffers, filters, etc. for application specific needs. The signal conditioner module can also be used to provide application specific connector needs. For example, the multi-wire profile monitor system will likely use multi-pin connectors while the loss monitor system might use BNC connectors. Providing this capability within a simple signal conditioner module prevents the need to design several similar ADC daughter cards.

Power Supply

A dedicated power supply for each common platform chassis will be provided. The exact details for this power supply are still being developed.

Chassis

Each common platform chassis will include one power supply, one carrier module and up to 2 daughter cards. The chassis will be 19" rack mountable and will typically be 2U in height. Some assemblies may require a larger height to accommodate the necessary panel space for connectors. For example, a 32-channel ADC daughter card with 32 BNC connectors, as planned for the beam loss monitor system, will require a height of more than 2U.

Cooling

As shown in Fig. 3, several small fans are planned to be used to provide cooling across the carrier module and daughter cards.

SYSTEMS TO BE SUPPORTED

The beam instrumentation systems that are planned to be supported by the common platform hardware include the following:

- Beam position monitor systems (BPM)
- Beam Loss monitor systems (BLM)
- Multiwire beam profile systems
- Beam current and charge monitoring systems
- Ionization Profile Monitor systems (IPM)
- Tune measurement systems
- Transverse injection damper systems
- And more

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The following sections provide preliminary system architecture details related to how the primary instrumentation systems will be supported using the common platform hardware.

Beam Position Monitors

A block diagram of the BPM daughter card is shown in Fig. 5. The EIC BPM system requirements require different filters and different data acquisition modes for each of the major subsystems. A common filter footprint will be designed to accommodate the different filter requirements using one common printed circuit board (PCB).

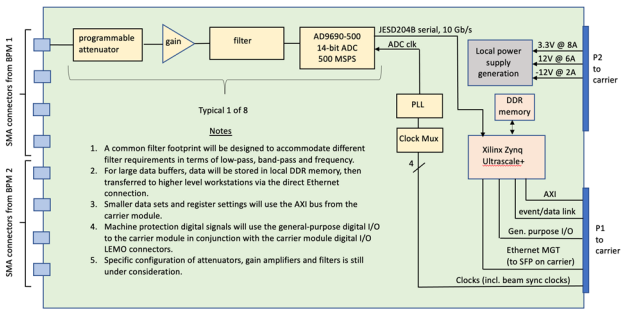

Figure 5: Block diagram of BPM daughter card.

The AD9690-500, 500 MSPS, 14-bit ADC is presently being considered for the BPM system, but further evaluation is required before making a final decision. This ADC uses the high speed JESD204B serial link (10 Gbit/s) for data transfer to the Ultrascale+ SoC.

The direct Ethernet connection to the Xilinx Zynq Ultrascale+ SoC will provide options for data to be sent directly to higher level workstations, bypassing the FPGA on the carrier module. Running Linux or other operating system directly on the on-board SoC is also an option, which would allow an EPICS IOC or RHIC Controls ADO to reside on the daughter card.

Tune Measurement and Transverse Injection Damper Systems

The tune measurement and transverse injection dampers systems will use the BPM daughter card, but with custom firmware to synchronize beam kicks and measurements.

The present plan is to provide beam kicks to a stripline via high voltage Behlke switches or similar.

Multiwire Profiles, Beam Loss Monitors, and Ionization Profile Monitor Systems

A general purpose 32-channel, 16-bit 5 MSPS analog input daughter card is presently being developed to accommodate a variety of system needs, including multiwire beam profiles, BLM and IPM systems (Fig. 6).

Each system will include custom firmware for the specific application, as well as a custom designed signal conditioner module to provide the specific front-end filter and external connector needs.

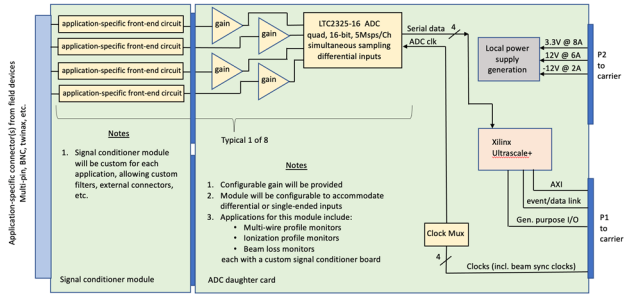

Figure 6: Block diagram of 32-chan 5 MSPS daughter card.

Beam Current and Charge Monitor Systems

For DC beam current measurements, DC Current Transformers (DCCT) and Faraday Cups will use a high-precision Analog Input/Output daughter card (Fig. 7). The daughter card will include low noise high bit count ADC and DAC components. The DAC output will generate a remotely configurable current source for the calibration of the DCCTs and other current transformers. This daughter card is still in the early design phase, and the specific ADC and DAC still need to be selected.

For bunch charge measurements (Wall Current Monitors (WCM), Integrating Beam Current Transformers (ICT), and Fast Current Transformers (FCT), etc.) another custom daughter card similar to the BPM module will be developed, but with DC coupled inputs and 1 GSPS or faster ADCs. This module is also in the very early design phase.

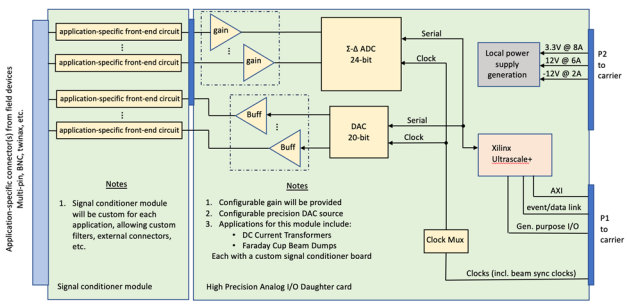

Figure 7: Block diagram of precision ADC/DAC daughter card.

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