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APS UPGRADE RADIATION SAFETY BEAM CURRENT INTERLOCK*

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Abstract

The Advanced Photon Source upgrade (APS-U) replaces the APS storage ring with a new Multi-Bend Acromat (MBA) storage ring utilizing on-axis swap-out injection requiring up to 20 nC charge per injected electron bunch, more than a three-fold increase from the original ring. Enforcement of radiation safety limits for the new storage ring will be accomplished by a new beam charge monitor interlock that acquires the accumulated beam charge in the Booster-to-Storage ring (BTS) transfer line and disables injection when the charge limit over a pre-set time period is exceeded. The new interlock is based on the existing APS Beam Shut-Off Current Monitor (BESOCM) that has been in operation in the APS injector for many years and incorporates significant improvements over the existing system. New features include use of direct digitization and FPGA processing, extensive remote monitoring capabilities, expanded self-test and fail-safe functions, and the ability to adjust settings and monitor status remotely via EPICS. The new device integrates a test pulse (self-check) feature that verifies the integrity of the integrating beam current transformer (ICT) and cable system used to detect the beam signal. This paper describes the new BTS interlock (BESOCM) design and presents results of bench test and in-machine evaluation of the prototype and production units.

INTRODUCTION

The existing APS BESOCM system limits the amount of accelerated charge in the APS Linac over a 1 minute accumulation period in order to enforce radiation safety requirements. If the limit is exceeded, the BESOCM disables the beam by inhibiting several necessary systems. The BESOCM continually tests itself by creating a single test pulse of ~2.5 nC after every beam trigger and sending the pulse through a test winding in the current transformer in the beam line, and has some addition fail-safes that monitor the trigger and integration gate [1,2].

The new BTS BESOCM will function similarly to the legacy system, but with far more adjustments and self-test functions, and will include robust remote monitoring capabilities.

APS ACIS System

The APS Access Control and Interlock System (ACIS) includes both personnel protection and radiation safety interlocks that act to disable accelerated and/or stored beam for a variety of abnormal conditions. The system uses dual redundant chains denoted A and B, and relies on fault tolerant hardware such as relay contacts and PLCs. The BTS BESOCM electronics chassis contains two redundant sets of electronics that interface to the ACIS system via safety rated relays.

APS Radiation Safety and FPGA Development

APS radiation safety requirements are stated in APS safety assessment documents and specify the risks and consequences of off-normal beam loss events [3]. Since the BTS BESOCM is a layer of protection added as part of the MBA upgrade, the FPGA firmware development process followed a graded approach based on the low specified risk, i.e., identical hardware was used in both chains A & B with separate firmware developers for each chain. Each developer worked independently to implement the FPGA functions as defined in the BESOCM engineering specification document. Independent code reviews were also performed on each FPGA code design.

BTS BESOCM SYSTEM DESIGN

Figure 1 shows a block diagram of the BESOCM system. The electron beam bunch charge is sensed by an Integrating Current Transformer (ICT) in the BTS beam line. The ICT has two independent identical test windings that allow beam to be simulated by passing a test pulse through the winding. One test winding is always in use during BESOCM operation, to provide the self-test pulse to the ICT. The second winding is used only during validation or testing. The ICT connects to the BESOCM electronics chassis, located outside the beam tunnel, via three coax cables.

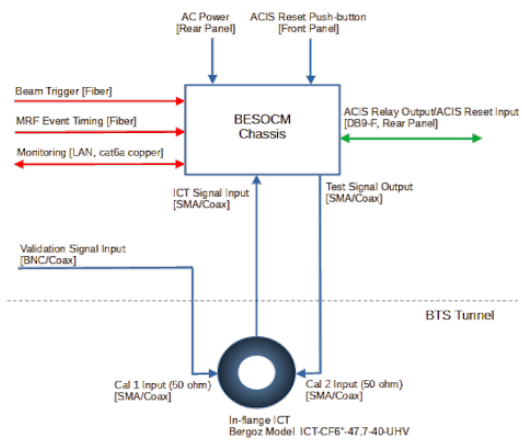

Figure 1: BESOCM system block diagram.

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The BESOCM performs the following measurements on each electron bunch, and will trip ACIS if any are outside preset limits:

- Accumulated beam charge
- Single beam bunch charge
- Beam timing

Correct beam timing is determined by comparing the arrival time of a detected bunch to the expected window based on the timing of the external trigger.

For each of three test pulses, the following checks are performed, and if the result is outside preset limits, a fault is generated:

- Pulse charge (integration)
- Pulse amplitude (peak)
- FWHM
- Baseline

In addition to beam and test pulse generated faults, the BESOCM has several system fail-safes faults (see Table 1).

Table 1: Fault Conditions

Fault #	Condition
1	Beam Pulse High
2	Beam Accumulator High
3	Beam Baseline Integrity
4	Test Pulse 1 Fail
5	Test Pulse 2 Fail
6	Test Pulse 3 Fail
7	CRC Bad
8	Charge Outside Window
9	Power Bad
10	ADC Saturation
11	Keylock in Program
12	Force Trip
13	ACIS Reset Hold-off
14	No Clock
15	reserved
16	No Trigger

Any fault will trip the ACIS relay to the unsafe state and latch until reset. The reset can only be accomplished manually, either by pressing the front panel reset button or via a remote reset signal input on the ACIS DB9 connector (see Fig. 1). The BESOCM front panel provides an LED indicator for each of the faults listed in Table 1. An EPICS PV is also available for each fault for remote monitoring.

Integrating Current Transformer (ICT)

The ICT is located in the BTS beam line (see Fig. 1). It outputs a gaussian-like pulse in response to a beam bunch passing through it; the area under this pulse is proportional to the bunch charge. The ICT is designed to output a pulse of at least ~20 ns width, even for very short beam pulses, resulting in a signal bandwidth below a few tens of MHz. Therefore, direct digitization of the ICT signal is achievable with reasonable sample rates. We used a 200 Msps, 16-bit ADC for the BESOCM design (LTC2107). The ICT is available from the manufacture with an optional test winding. We requested a custom ICT design with two test windings to allow for validations to be performed without impacting the self-test function.

As in our existing BESOCM system, a single ICT is used for both chains; each chain independently analyses the self-test pulses to provide redundancy. In response to our request, the ICT manufacturer (Bergoz) performed failure testing of ICTs by creating various failure conditions and recording the effects on the ICT response. The results demonstrate that the BESOCM self-test pulse function will detect ICT failures such as windings shorted or open, internal component failures, etc. This testing provided additional justification for using a single common ICT for both chains [4].

BESOCM CHASSIS DESIGN

The BESOCM chassis (see Figs. 2 and 3) contains several circuit boards:

- FPGA Processing Boards (A & B)
- Test Pulse Generator Board
- ICT Buffer and Fan-out Board
- ACIS Interface (Relay) Board
- Power Supply Distribution Board

A brief description of each board is given below.

Figure 2: BESOCM chassis, front view.

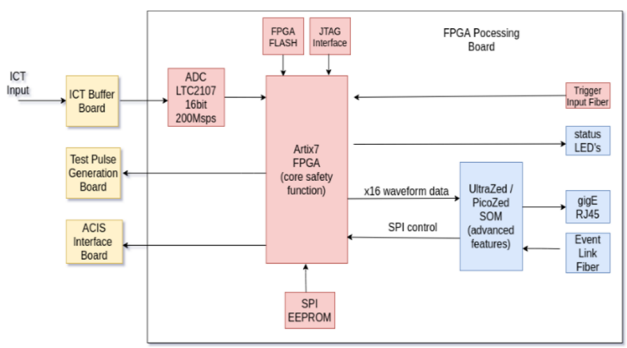

Figure 3: BESOCM chassis components block diagram. The components inside the border are duplicated for each of the two chains.

FPGA Processing Board

The FPGA processing board includes the Artix 7 FPGA, the ADC that digitizes the ICT signal, ACIS latch circuit,

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watchdog ICs that monitor timing signals and power, and connectors to mount the PicoZed SOM modules. The board provides I/O connections for the PicoZed LAN, USB-serial and MRF event receiver external connectors on the front panel.

Test Pulse Generator Board

The test pulse generator board schematic is shown in Fig. 4. The circuit generates up to four different test pulses that are sent to the test winding of the ICT via a coax cable to simulate beam pulses of varying charge. The pulse is selected using a fast analog switch controlled by the FPGA. The charge level of each pulse is set by a fast MOSFET along with an attenuation network and DC block. For each pulse, the FPGA provides two timing signals that control the delay and width of the pulse. The pulse width adjustment allows control over the resulting pulse charge. The MOSFET produces a small but significant transient pulse; the adjustable delay allows the test pulse to be positioned such that it combines with the switch transient, effectively eliminating it as an issue [5].

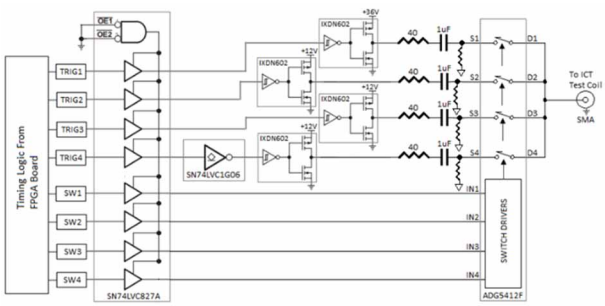

Figure 4: Test pulse generator circuit.

The BESOCM is configured to use three test pulses in sequence that cover the operating range of the ADC.

ACIS Interface Board

The ACIS interface board has two safety-rated relays that provide the interface to the ACIS system chains A & B via a DB9 connector on the BESOCM rear panel. This board also includes a reset relay with an externally driven coil that resets the fault latches in the same manner as the front panel reset switch, allowing operators to reset faults remotely from the control room.

SYSTEM SETTINGS AND MONITORING

EPICS IOC

The PicoZed SOM daughter boards run Ubuntu Linux. Each board implements an embedded EPICS IOC that provides process variable (PVs) for all settings and readbacks, including waveforms.

CSS GUI Screens

Extensive Control System Studio (CSS) engineering screens were developed by the BNL team. The screens allow monitoring of the BESOCM in real time and include digitized waveforms of the beam ICT output and the three test pulses along with test parameter measurement results on the waveforms. Plots of the accumulator and beam history for the previous hour are displayed, along with live and latched fault status. Power supply voltage and current, and board temperatures are also displayed. Separate screens for the beam pulse, and each test pulse, with more detailed analysis are available, along with a post-mortem screen that saves BESOCM data at the time of the last fault (see Fig. 5).

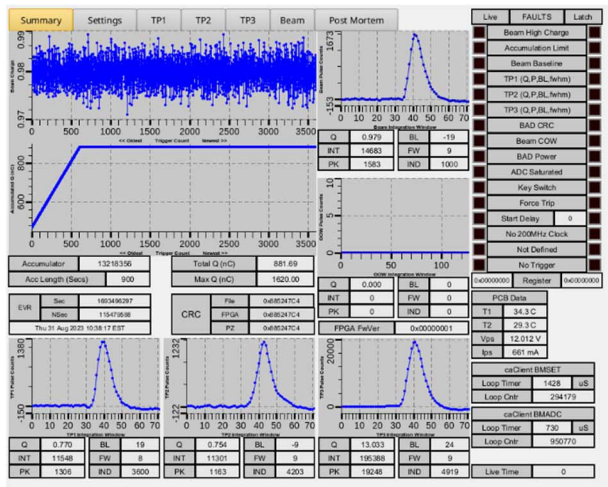

Figure 5: Engineering Summary screen; tabs provide access to other screens with more detailed information.

Changing System Settings

The BESOCM stores the system settings in a flash EEPROM on the FPGA main board, along with a CRC hash. Upon power up, the settings and CRC are transferred to FPGA memory. During operation the BESOCM continuously re-calculates the CRC on every 1 Hz trigger to ensure the integrity of the settings data.

The EPICS IOC provides PVs for all the settable parameters, such as accumulation time, beam limits, test pulse limits and timing, beam charge calibration, etc. As all these settings are critical to the BESOCM function, strict control over any changes to the settings is required. Therefore, we implemented a hardware enable using a key switch on the front panel that enables or disables writing to the EEPROM. When the BESOCM is in its normal operating mode, the key switch is in the "run" position which prevents any data transfer into the EEPROM. When the key switch is set to "program" writing to the EEPROM is enabled and an ACIS trip state is always asserted. This prevents beam from being transferred through the BTS line. APS administrative controls require the BESOCM to be re-validated after any switch to "program".

The CSS Settings screen is shown in Fig. 6. The screen is divided into three sets of equivalent PVs. The top set is the editor; the middle set displays the contents of the settings file; the bottom set displays the FPGA values. The buttons on the right control the transfer of settings from the editor to the FPGA via the settings file and flash EEPROM. Changes can only occur when the front panel keylock is set to "program". The editor section allows

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settings to be written to and read from the settings file. The settings file is used to temporarily store the settings; in normal operation only the FPGA values are relevant. Any discrepancy in the value of a setting between the three sections is highlighted in red (not shown). The red boxes on the right indicate the key switch is in "run" mode.

Figure 6: The Settings screen.

EVALUATION AND TESTING

Three production units have been delivered to APS from BNL. Each unit has been tested and evaluated in the lab with simulated beam without issues. One unit was installed in the BTS during the final APS run and performed as expected. Once the upgraded BTS beam line is operational, we plan to do extensive statistical analysis with real beam to determine the best settings for the various fault limits with different beam charge, timing, etc., with the goal of ensuring maximum fail-safe function and minimal interruption to operations from spurious trips.

VALIDATION

APS requires annual re-validation of safety systems. We are currently developing a new validation procedure for the BTS BESOCM that will test and validate each of the beam and self-test fault functions. The extensive EPICS PVs will aid in automating the new validation procedure.

CONCLUSION

In preliminary testing and evaluation, the BTS BESOCM has operated reliably and is a significant advancement over the existing BESOCM system. We are preparing to install it in the upgraded BTS line and expect it to be fully operational when the upgraded BTS line is commissioned.

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